AstroPix – A novel HV-CMOS pixel sensor for space-based experiments

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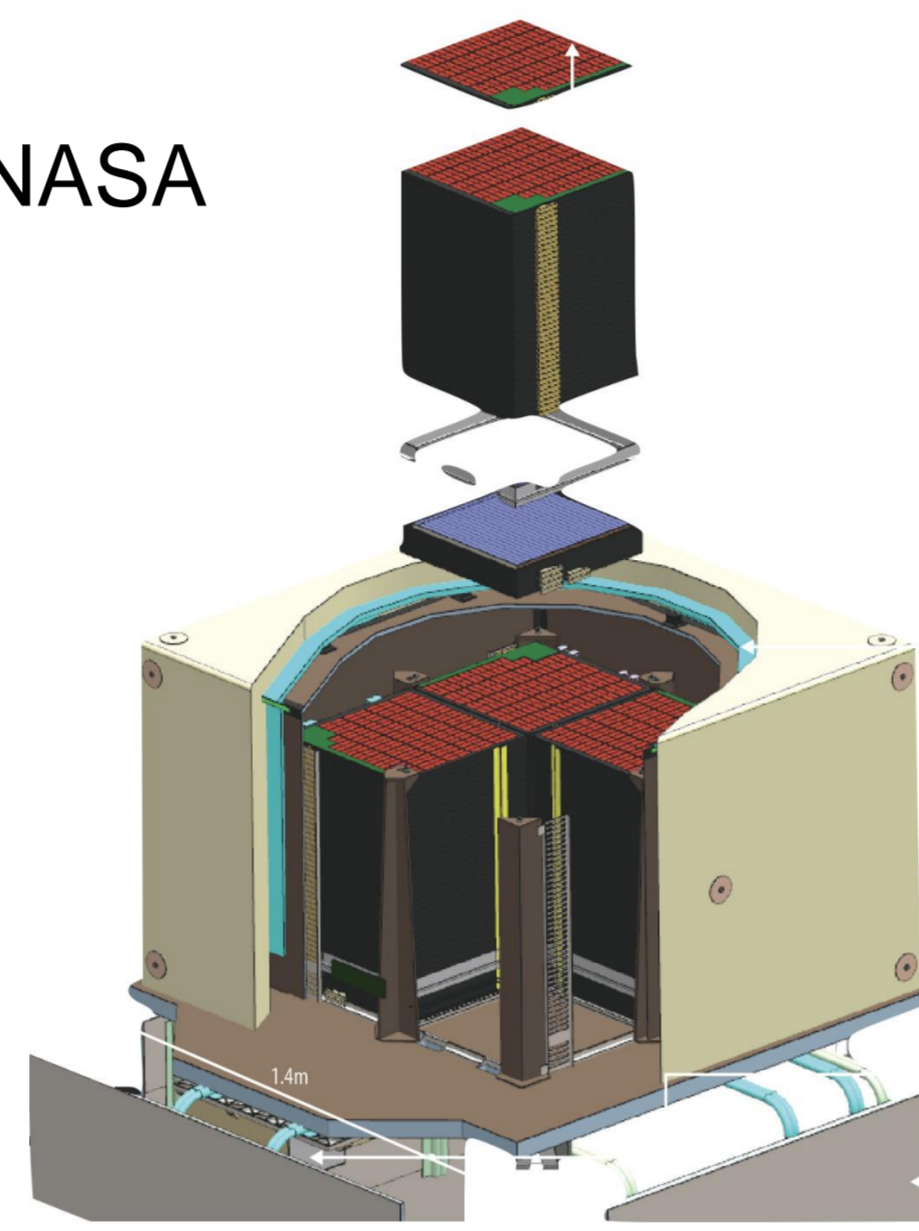
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Motivation: Gamma-ray Astrophysics

- Developed for AMEGO-X mission concept proposed by NASA
- Multi-messenger astronomy
- HV-CMOS based Tracker:
  - 4 Towers with each 40 layers
  - 64000 sensors and 25 m^2 active area

Requirements:

- Fully depleted 500 um thick sensors
- Low power 1.5 mW/cm^2
- High dynamic range 20 – 700 keV

Caputo, R. et al.
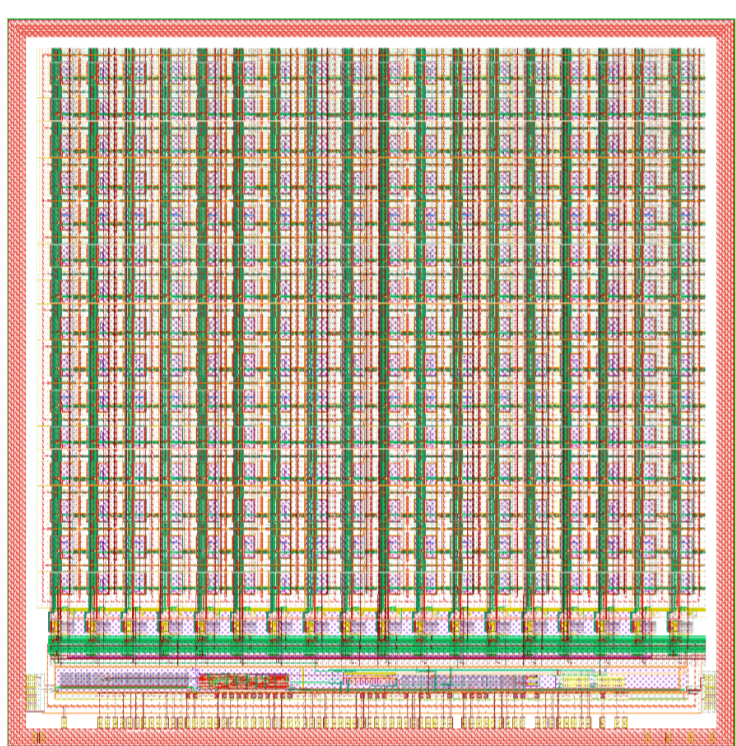"The All-sky Medium Energy Gamma-ray Observatory eXplorer (AMEGO-X) Mission Concept"

AstroPix3: First full reticle size prototype

- Implemented in TSI 180 nm process
- Submitted in May 2022
- Chip size: 2 cm × 2 cm
- Pixel matrix: 35 columns, 35 rows
- Pixel size: 300 μm × 300 μm
- OR'd row/column-based readout
- ToA: 8 bit counter (2.5 MHz external clock)
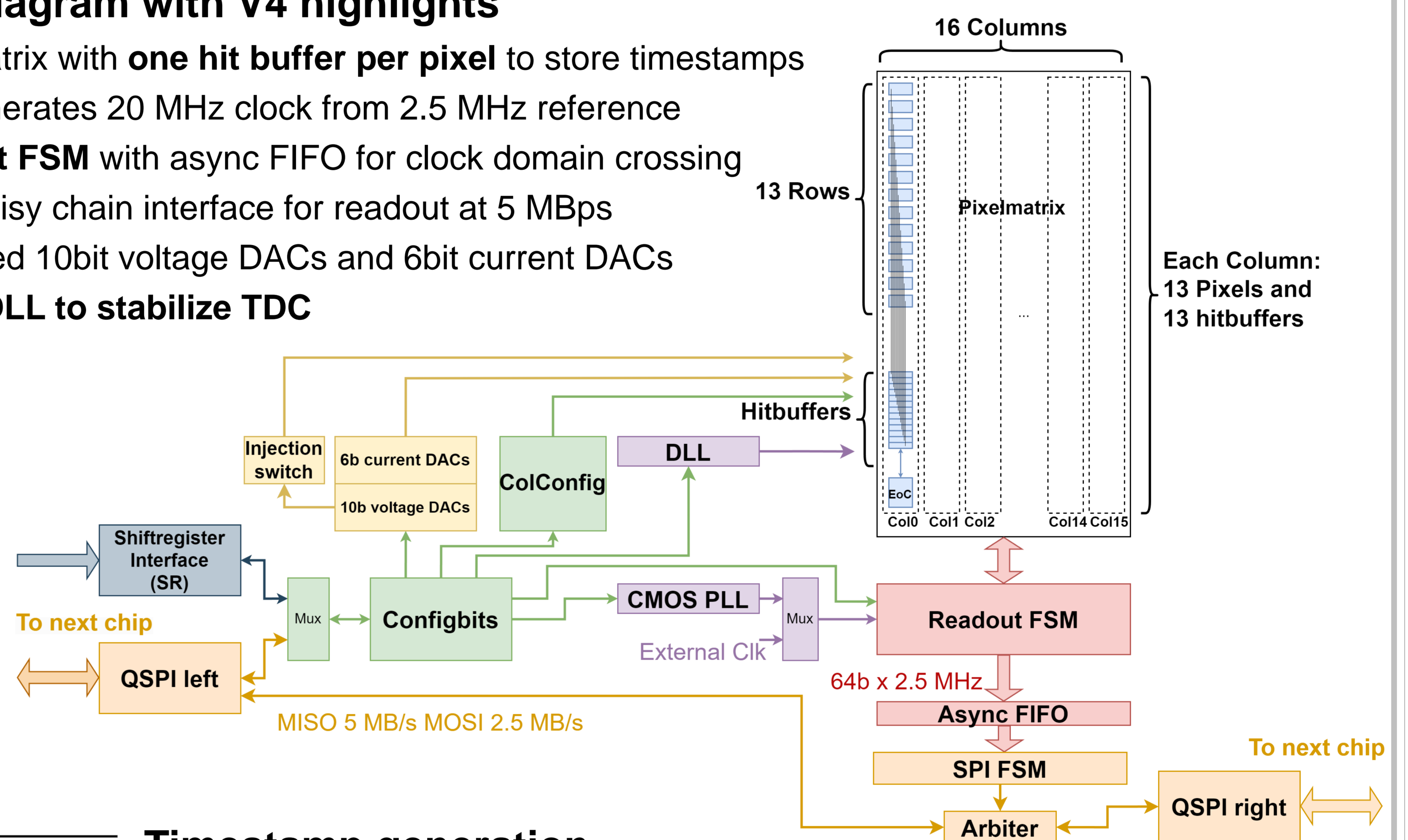- ToT: 12 bit counter (200 MHz external clock)

Currently being characterized

AstroPix4

Specifications

- 1 × 1 cm^2 chip in TSI 180nm process
- Pixel matrix: 16 columns, 13 rows
- Pixel size: 300 μm × 300 μm
- Pixel pitch: 500 μm

Improvements over V3

- Per-pixel readout architecture
- Reduced pixel capacitance by 30%
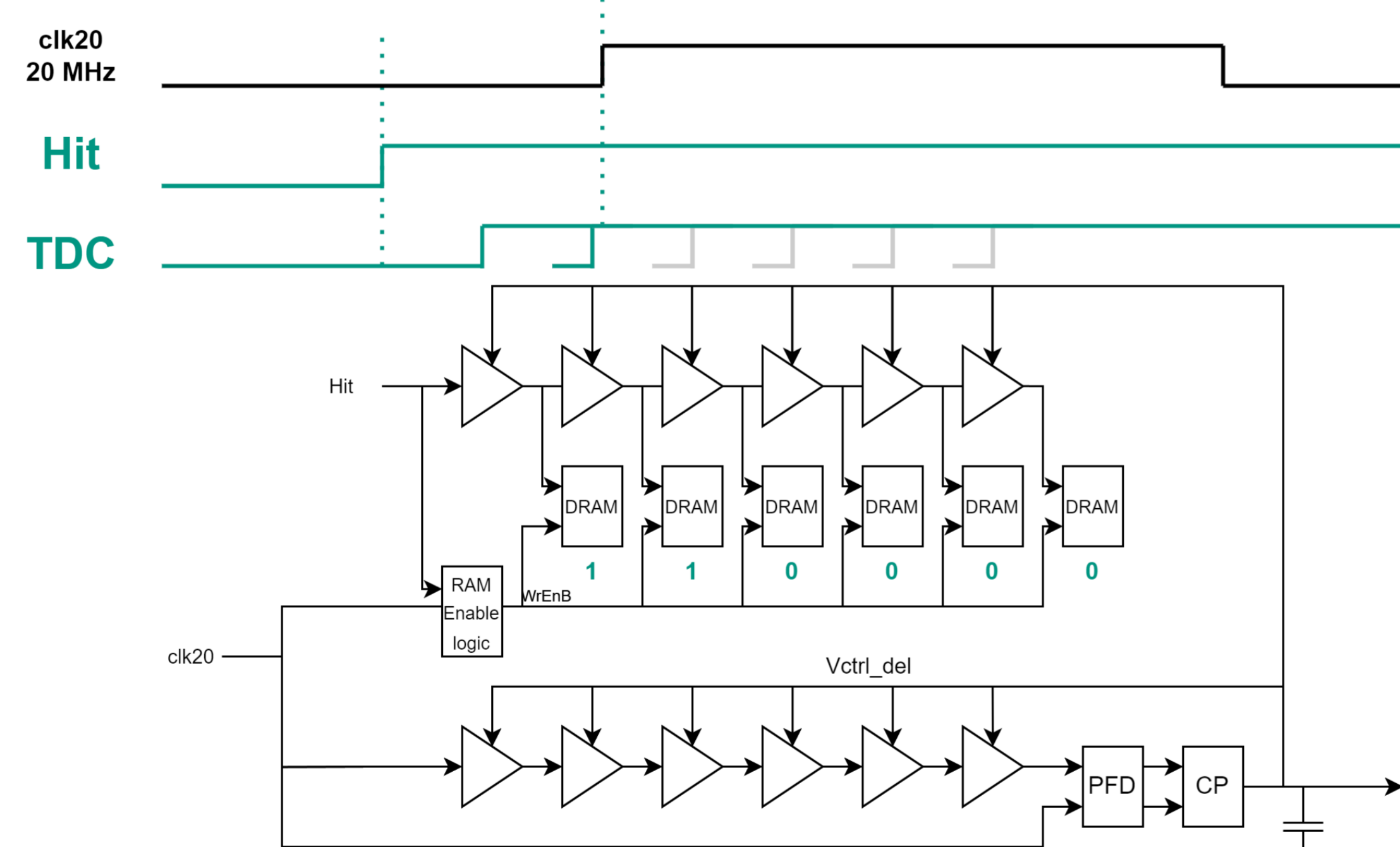- 3 bit TuneDAC per pixel

Block diagram with V4 highlights

- Pixel matrix with **one hit buffer per pixel** to store timestamps
- **PLL** generates 20 MHz clock from 2.5 MHz reference
- **Readout FSM** with async FIFO for clock domain crossing
- QSPI daisy chain interface for readout at 5 MBps
- Integrated 10bit voltage DACs and 6bit current DACs
- Global **DLL to stabilize TDC**

16 Columns

13 Rows — Pixelmatrix

Each Column: 13 Pixels and 13 hitbuffers

Hitbuffers

EoC — Col0 Col1 Col2 ... Col14 Col15

Injection switch — 6b current DACs — 10b voltage DACs — ColConfig — DLL

Shiftregister Interface (SR)

To next chip — QSPI left — MISO 5 MB/s MOSI 2.5 MB/s

Mux — Configbits — CMOS PLL — Mux — Readout FSM

External Clk

64b x 2.5 MHz — Async FIFO — SPI FSM — Arbiter — QSPI right — To next chip

Timestamp generation

- Coarse timestamps saved in DRAM at leading and trailing edge of a hit
  - 17 bit x 20 MHz generated by global counter
  - 1 bit x 20 MHz negative edge timestamp
- 17 bit Flash-TDC measures time from both edges to next rising clock edge with 3 ns resolution
  - Delay elements based on two current starved inverters
  - Connected to DRAM cells
  - 50 ns total delay controlled by global DLL

clk20 20 MHz — Hit — TDC

Hit — DRAM 1 — DRAM 1 — DRAM 0 — DRAM 0 — DRAM 0 — DRAM 0 — wEnB

RAM Enable logic — clk20 — Vctrl_del — PFD — CP

Summary

- Submitted new AstroPix4 design in May 2023, currently in production
- Should fulfil AMEGO-x requirements, plan to build balloon prototype (ComPair)
- Improved time-of-arrival resolution from 400 ns and ToT resolution from 5 ns to 3 ns
- Reduced module complexity and power consumption by removal of ext. 200 MHz ToT clock
- Implemented per-pixel readout and tuning capability

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