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AstroPix: A novel HV-CMOS pixel sensor for space-based experiments

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A new application for monolithic pixel detectors is NASA's AMEGO-X project [1], which is a low-orbit gamma ray observatory for multimessenger astrophysics, proposed as a 3 to 5 year mission. For the 40-layer gamma-ray telescope, which will consist of over 64000 sensors with a total area of more than 25 m², a new low power < 2 mW/cm² and high dynamic range 20–600 keV monolithic active pixel sensor with 500 μm depletion thickness, named AstroPix, is currently being developed.

Summary (500 words)

The first two versions, AstroPix1 a 5 x 5 mm² test chip with 18 x 18 200 x 200 μm² pixels and AstroPix2 a 1 x 1 cm² test chip with 35 x 35 250 x 250 μm² pixels have already been designed and fabricated in TSI's 180nm process. The energy resolution and the SEU and latchup performance required for the usage in space are currently studied in test beams [2]. The newest version AstroPix3, has been submitted for fabrication in July 2022 and received back in January 2023.

This prototype is the first full reticle chip with 300 x 300 μm² large pixels and a 500 μm pitch. It features a new guard ring design expected to withstand a reverse bias of over 300 V, which is needed to reach the required 500 μm depletion thickness on a > 10kOhm-cm resistivity substrate.

The AMEGO-X tracker will consist of 4 towers with 40 layers, each embedding 20x20 pixels. To simplify the module construction, AstroPix features a daisy-chain QSPI interface, which allows chip-to-chip readout and configuration, occupying only 5 data lines per SPI-bus on the DAQ for multiple chips. All bias currents and voltages need are internally generated by 6-bit current and 10-bit voltage DACs. The analog in-pixel front-end consists of a charge-sensitive amplifier implemented as n-type cascode amplifier with an additional feedback capacitance to increase the dynamic range, a band-pass filter, and a CMOS comparator converting the analog pulse to a digital signal. Pixels are or'd in row and column, to reduce the number of readout channels to the sum of rows and columns. To reduce crosstalk between the long metal traces connecting the pixel and the synthesized digital logic in the bottom periphery of the chip, the or'd signal is level shifted to a reduced amplitude.

In the periphery, a global timestamp generated by an 8-bit counter driven by an external 2.5 MHz timestamp clock is assigned at the leading edge of the hit. At the same time the ToT is measured by a 12-bit counter driven by an external 200 MHz clock. The readout via SPI is only triggered, if there is data to be read out i.e. an open-drain signal connected to all the chips on one bus is pulled low, to keep the active duty-cycle of the SPI interface low.

A new version AstroPix4 is currently in submission, which removes the or'd readout and implements a per-pixel readout, while at the same time reducing the power consumption by replacing the fast counter-based ToT measurement by a Flash TDC based method, resulting in a very low power consumption given the low duty cycle of 10-5 and an improved time resolution of 3.125 ns for timing and ToT. The integration of a PLL reduces the number of connections to the DAQ to one 2.5 MHz reference clock and the SPI lines.

The design and first measurements of AstroPix3 as well as the development of AstroPix4 will be presented.

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