Design and measurements of SMAUG1, a prototype ASIC for voltage measurement using noise distribution

Grzegorz Wegrzyn, Robert Szczygiel – AGH University of Krakow, Poland
Contact: wegrzyn@agh.edu.pl

TWEPP 2023, Geremeas, Sardinia, Italy

AGH UNIVERSITY OF KRAKOW

Introduction

In this work, we present the design, test system, and preliminary measurements of SMAUG1 - a prototype ASIC, implementing an algorithm of indirect voltage measurements using distribution of the signal noise. The ASIC is a prototype of X-ray imaging, pixelated system with eight 16-bit counters in each pixels.

Implementation requirements

The algorithm introduces additional requirements for the implementation:

- At least 3 measurement points (because of 3 unknown of fitted curve: mean, deviation and scale),
- The distance between adjacent threshold levels should be comparable to noise sigma (in our case: ~1mV),
- High-speed comparators with minimized hysteresis (less than sigma noise <1mV),
- Equally fast comparators
- CSA working in charge-mode

Test setup

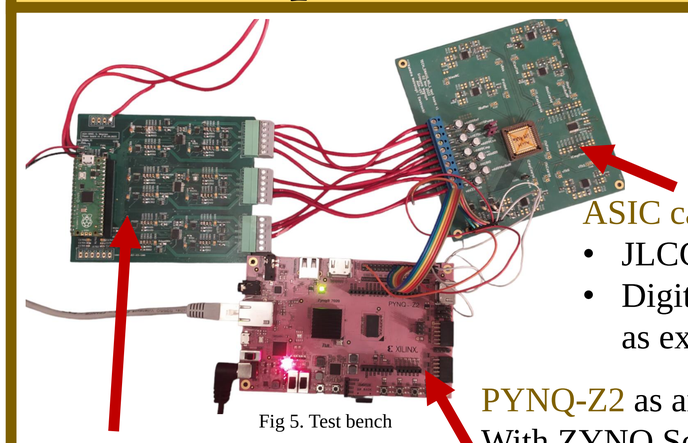

Fig 5. Test bench

ASIC carrier board:

- JLCC44 slot
- Digital potentiometers as external biases

PYNQ-Z2 as an executive unit. With ZYNQ SoC, provides custom logic feature with implemented: I2C, SPI, GPIO and DTC. Used for conducting tests and processing data.

Power board in 2 different options: with LDOs and DC-DC provide easy to use powering with voltage and current control.

Implemented algorithm

The test algorithm uses multiple comparison levels, distributed close to the expected signal amplitude, to measure the noise distribution of a signal. During the measurement, the signal with the noise is crossing threshold levels (see the figure on the right). The number of these events and threshold level values gives points to which the distribution curve fits. The mean value of the fitted curve is the signal amplitude. [1]

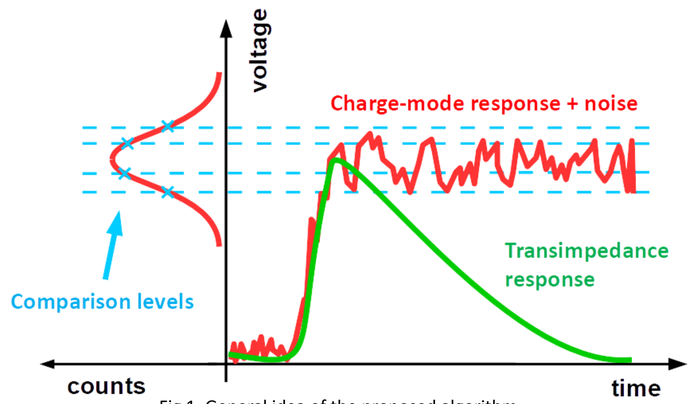

Fig 1. General idea of the proposed algorithm

ASIC Design

The designed ASIC contains an SPI interface, bias circuits, and a 7x7 matrix of pixels with 68x68µm size. There are CSA, 8 comparators grouped into 2 groups, and trimming DACs within each pixel. Each comparator has internal DACs to trim its current and fine tune its threshold. Grouping comparators into 2 groups stems from coarse threshold tuning which is independent for each group. As it is the first prototype, there is no possibility of mounting a detector. We implemented a simple calibration circuit, instead.

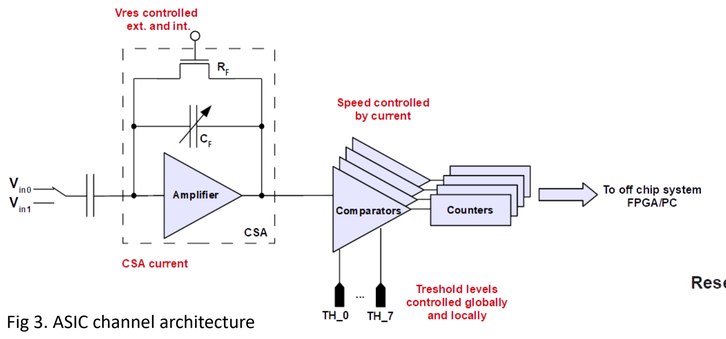

Fig 3. ASIC channel architecture

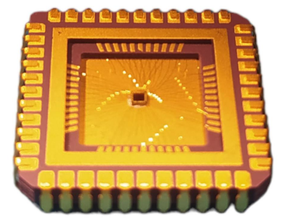

Fig 2. SMAUG1 in JLCC44 package

Key parameters (simulations):

- gain: 150 mV/fC (5.5fF)
- noise: 2.5mV (ENC: 95e)

AMUX with buffer allow to check internal DACs and key nodes inside the chip.

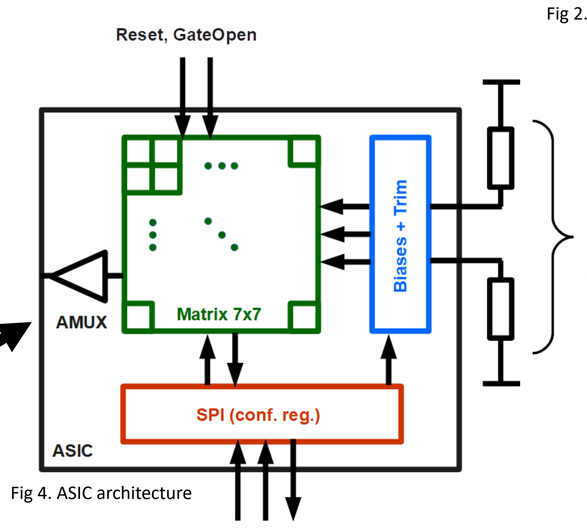

Fig 4. ASIC architecture

Measurements

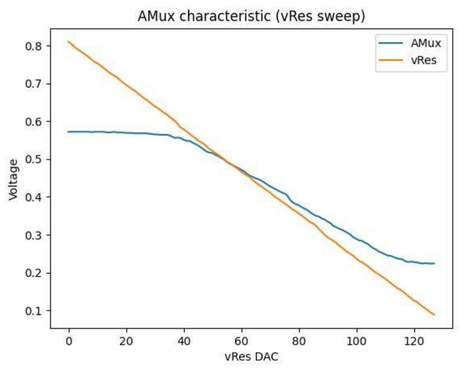

Fig 6. AMUX dynamic range

Very first measurements shows problems with dynamic range of a buffer of the AMUX. Based on simulations it should be ~850mV less than power supply. Measured range is ~400mV.

Measured noise is very close to simulated one. Noise sigma extracted from noise occupancy scan is in range 1.7 - 2.5 mV depends on channel and sample.

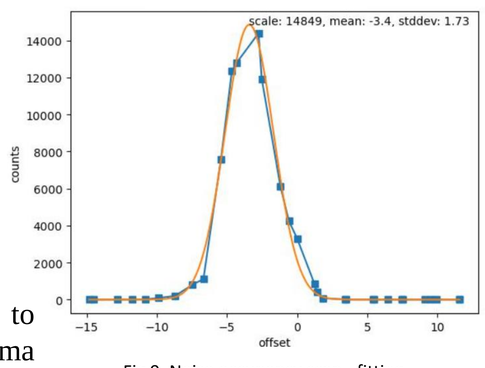

Fig 9. Noise occupancy scan - fitting

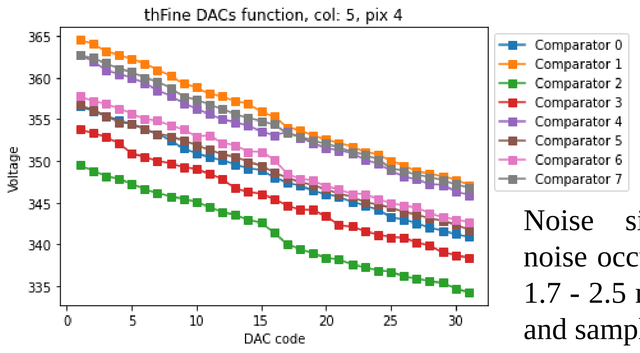

Fig 10. DACs characteristics

Noise sigma extracted from noise occupancy scan is in range 1.7 - 2.5 mV depends on channel and sample.

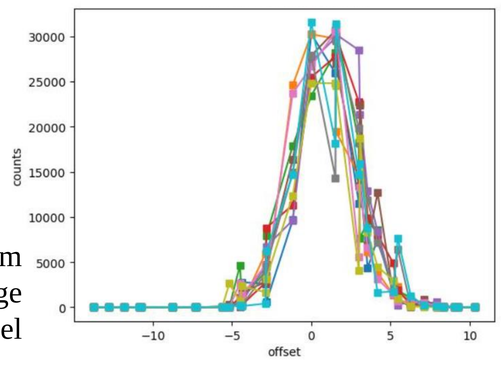

Fig 9. Noise occupancy scan - repeatability

Further works

Improve test setup to minimize the influence of the external noise sources. Then we will able to conduct the final tests.

The second prototype SMAUG2 is in development. In this prototype we would like to fix all issues (amux, DACs) found in the first chip. We have also foreseen new features e.g. conducting measurements with CSA in the transimpedance mode.

Bibliography

1. Grzegorz Wegrzn and Robert Szczygiel. *Voltage measurements using noise distribution*. Przegląd Elektrotechniczny, pages 161–163, 2021.

Acknowledgements

The work was supported by the Polish Ministry of Science and Education (contract no.0138/DIA/2020)