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Design and measurements of SMAUG1, a prototype ASIC for voltage measurement using noise distribution

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In this work, we present the design, test system, and measurement results of the SMAUG_ND_1 ASIC. The described circuit implements an indirect energy measurement algorithm based on noise distribution measurement. The algorithm is similar to the threshold scan procedure but is done with a single pulse. The chip implements the matrix of 7x7 pixels each with 8 independent comparators and a size of 75x75um. The work describes the measurement process and the results of the algorithm as well as a brief discussion of what can be improved in the next version of the ASIC.

Summary (500 words)

SMAUG_ND_1 is a prototype ASIC, developed in CMOS 28nm technology, which is designed to test the algorithm for voltage measurement using a noise distribution. This algorithm is similar to the threshold scan procedure. The main difference is that it is performed on a single pulse instead of a series of pulses and simultaneously utilizes multiple threshold levels. The idea is to fit the Gaussian curve to get a higher energy resolution than widely used $CR - RC^2$ filters with amplitude or ToT measurements. The tested algorithm was described in our previous work [1].

The main challenge was related to the accurate distribution of threshold levels which positions should be well known to be useful in the mentioned algorithm. Therefore we had to implement fine-tuning DAC within each comparator. The next possible source of errors is the difference between the speed of comparators, which also can be trimmed using dedicated DACs, separated for each comparator(fig 1.).

Another requirement was related to the charge-sensitive amplifier (CSA) which is used as the very first stage of the processing chain. CSA should work in charge integrating mode to provide a possible flat response, which will be easy to measure using the mentioned algorithm. Therefore as a CSA feedback, we used the simple transistor whose gate potential can be controlled by an external voltage source. At the time of measurement, the transistor is in the off state, and just after measurement, it can be easily turned into an active state to discharge the preamplifier. To minimize gate leakage currents that can discharge feedback capacitance we decided to use thick oxide transistors as an input transistor and in the feedback.

The chip provides 8 comparators in each channel to increase the accuracy of further Gaussian curve fitting. Comparators are divided into two banks with separated DACs for coarse tuning of the threshold. This allows the tested algorithm to be combined with correlated double sampling [2]. To increase the maximum counting rate, we have not implemented hysteresis in the comparators. Each discriminator is connected to a 16-bits ripple counter.

The initial measurements show a problem with the analog buffer, which has a very limited dynamic range compared to the simulation. Nevertheless, the available range is still sufficient to check the linearity of the internal DACs for fine-tuning the threshold (see fig. 2). The comparator's count rate measurement shows a relatively large mismatch (compare the height of the bars in fig. 3.), so if the comparator count rate trimming is not sufficient, normalization will be necessary.

The goal of the first prototype is to confirm if we can achieve the required parameters and check if the algorithm will work. At the time of writing this abstract, ASIC is under testing and final data is not yet available.

Detailed results will be reported at the time of the conference.

[1] - G. Wegrzyn, R. Szczygiel, “Voltage Measurement Using Noise Distribution”, 2021
[2] - W. Buttler et al. “Noise Filtering for Readout Electronics”, 1990

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