ETROC2: the first full size, full functionality Precision Timing ASIC prototype for LGAD-based CMS Endcap Timing Layer (ETL) Upgrade

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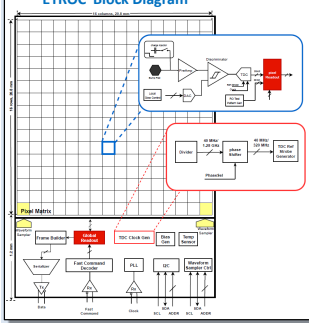
ETROC Block Diagram



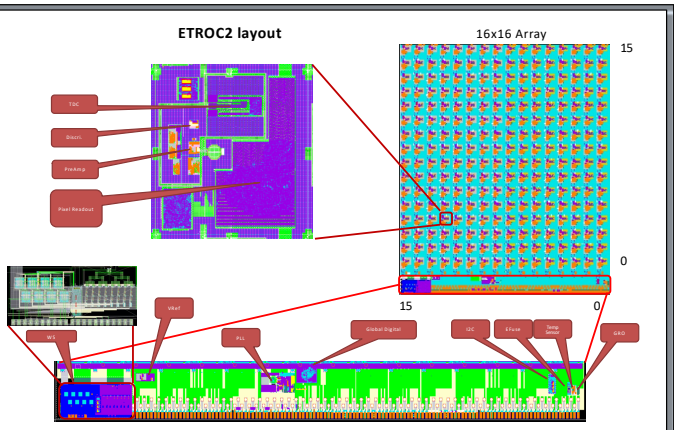
ABSTRACT

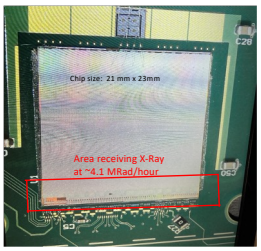
The **ETROC (Endcap Timing Readout Chip)** is being developed for the **LGAD-based CMS Endcap Timing Layer (ETL) at HL-LHC**. The ETL on each side of the interaction region will be instrumented with a two-disk system of MIP-sensitive LGAD (Low Gain Avalanche Diodes) silicon devices, read out by ETROCs for precision timing measurement with down to ~35 ps timing resolution. The ETROC is designed to handle a **16 x 16 pixel cell matrix**, with each pixel being **1.3 mm x 1.3 mm** to match the LGAD sensor pixel size. Approximately 15% of the sensors near the highest eta region will experience hadron fluence above 1e^15 neq/cm^2 towards end of operation of HL-LHC, resulting in small signal amplitude with reduced LGAD gain. For this reason, the front-end design for preamplifier and discriminator has been specifically optimized for the reduced LGAD signals, with enough flexibilities to meet the ETL specific needs for time resolution, power budget and radiation profile.

The ETROC chip is implemented in a commercial 65nm CMOS process. Each channel consists of a preamplifier, a discriminator, a TDC used for TOA (Time Of Arrival) and TOT (Time Over Threshold) measurements, and a memory for data storage and readout. An in-pixel auto threshold calibration is included, along with a self-testing pattern generator. The TOT is used for time-walk correction of the TOA measurement. The detailed hit information (TOA and TOT) from each cell will be read out from a local circular buffer after each Level-1 Accept (about 1 MHz). In addition, a charge injection circuit is implemented to allow for testing and calibration. For more detailed monitoring of the signal pulses as radiation dose increases, waveform sampling circuits are included for one pixel. The clock distribution is based on the ETROC1 4x4 H-tree design, scaled up to 16x16 with a new shielding structure added to alleviate potential interference. The global peripheral circuits include a PLL, a phase shifter, an I2C slave controller, a fast control block, a global readout, and a data driver along with an efuse and temperature sensor. The ETROC builds event data frames for each L1A selected event and is also capable of providing L1 trigger information for user-defined delayed hits. The main design challenge is how to extract precision timing information from the small LGAD signals in the presence of high irradiation fluence, while keeping the power consumption and digital activity low. The ETL design goal for the time resolution of 50 ps per hit is required to achieve a 35 ps arrival time measurement for a MIP particle, which has its track registered in two ETL disk layers. The LGAD contribution is known to be about 30 ps, this means that the jitter from the ETROC has to be kept below 40 ps.

The ETROC2 is the first full size (16x16) and full functionality prototype and its dimension is 21mm x 23mm, making it one of the largest chips in HEP.

ETROC2 layout



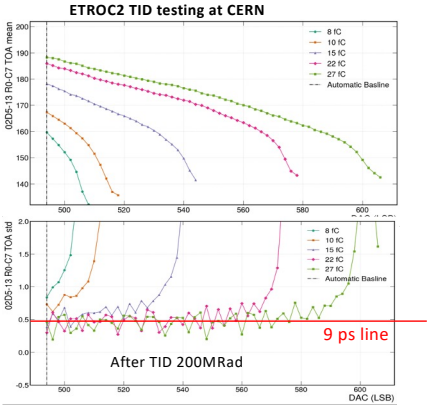


Temperature vs Voltage vs TID scan done at CERN in Aug 2023

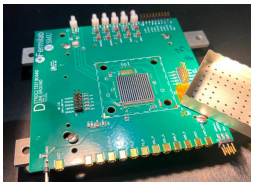
T: from -30C to +30C
V: from 1.3V to 1.0V
TID: to 200 MRad

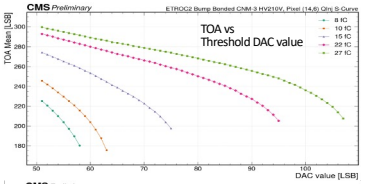
All works

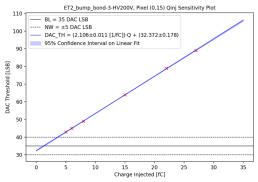
ETROC2 TID testing at CERN

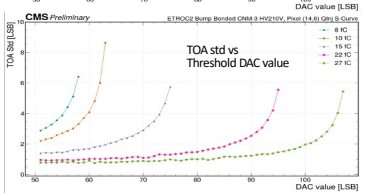


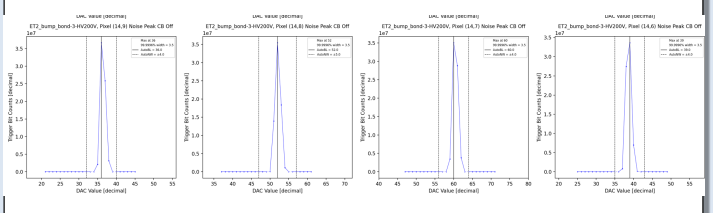
Bump bonded ETROC2 performance using charge injection





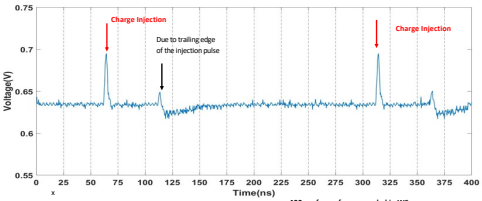






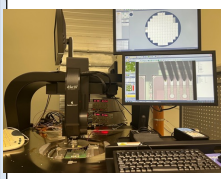
WAVEFORM SAMPLER (2.56 GS/s): recorded waveform using charge injection

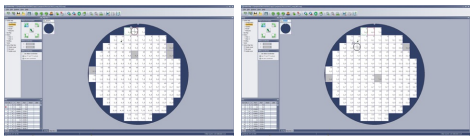
For the robust long term operation of the ETL it will be important to monitor signal waveforms to detect variations from the increasing radiation dose. Recorded waveforms can be used to optimize thresholds and bias voltages in order to maintain the target performance. The 10bit (Effective Number of Bits (ENOB)) 320MS/s ADC is the critical building block for waveform sampler for ETROC. ETROC can use a 2.56 GS/s wave sampler which interleaves 8 channels of the 320MS/s single-channel ADC.



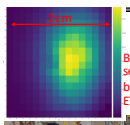
Wafer probe testing to study the yield at CERN in Aug 2023

Two new ETROC2 wafers from TSMC : The probe testing has showed 4 bad dies (out of 116 dies) per wafer in each case. Production QC procedure has been developed and established for wafer probe testing.

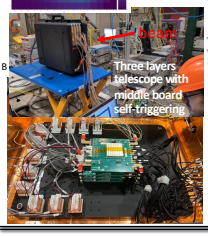


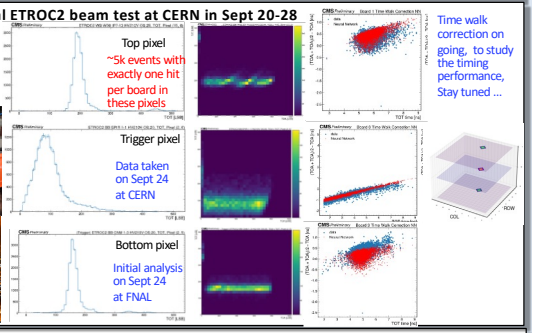


Initial ETROC2 beam test at CERN in Sept 20-28



Beam profile seen by bump bonded ETROC2+LGAD





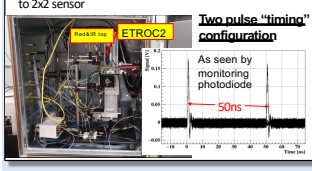
Time walk correction on going, to study the timing performance, Stay tuned ...

First look at ETROC2 performance with a double pulse IR laser at CERN-SSD (Sept 2023)

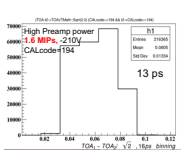
With ETROC2 wire-bonded to 2x2 sensor

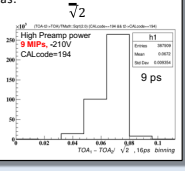
$$\sigma^2_{ToA} = \sigma^2_{laser} + \sigma^2_{Clock} + \sigma^2_{sensor} + \sigma^2_{ETROC2}$$

Jitter calculated as: $\frac{\sigma(TOA_1 - TOA_2)}{\sqrt{2}}$



Two pulse "timing" configuration





ACKNOWLEDGEMENT

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