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The first full size full functionality ETROC2 (16x16) prototype for CMS MTD Endcap Timing Layer (ETL) upgrade

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The Endcap Timing ReadOut Chip (ETROC) is designed to process LGAD signals with time resolution down to about 40-50ps per hit. The ETROC2 is the first full size (16x16) prototype design with the front-end based on and scaled up from the ETROC1 (4x4). The readout designs at pixel and global level and the system interfaces are all new and are compatible with the final chip specifications in terms of functionality. The ETROC2 is intended as a learning chip, as a stepstone to the ETROC3 which is intended as the pre-production design. The ETROC2 design and test results will be presented.

Summary (500 words)

The ETROC2 is the first full size (16x16) and full functionality prototype design and its dimension is 21mm x 23mm making it one of the largest chips in HEP. The analog front-end design (preamp, discriminator and TDC) for each pixel is based on the ETROC1 pixel design, while the pixel readout and global readout design is entirely new with a switch-cell based network approach. The bump bonded ETROC1 chips (with LGAD sensors) have encountered a noise originated from its own 40MHz readout clock and coupled via the bump bonded sensor into the preamplifier input. One of the main focuses of the ETROC2 design is to minimize this digital noise in order to reach low enough discriminator threshold to achieve the timing performance when LGAD gain is reduced due to irradiation towards the end of life at HL-LHC. The clock distribution is also based on the ETROC1 4x4 H-tree design, scaled up to 16x16 with a new shielding structure added to alleviate potential interference. The ETROC2 PLL is migrated from the clock generator block from lpGBT with metal stack change and some new blocks for calibration. A few new features have been added to the ETROC2, including a waveform sampler for the preamplifier output for one of the pixels for monitoring purpose, the on-chip and in-pixel auto discriminator threshold calibration, built-in self-testing capability with digital pattern generation within each pixel, as well as the capability to provide a coarse map of delayed hits continuously for every bunch crossing for monitoring or Level 1 triggering purposes. To minimize the risk from ETROC1 to ETROC2, a few dedicated testing chips were designed and carefully tested, including the rad-hard version of the waveform sampler chip, the ETROC-PLL chip which is based on the lpGBT PLL, and special I2C testing chip. In addition, the new pixel and global readout has been emulated in FPGA for design verification and testing purposes. The ETROC2 emulator has been tested with the rest of the system before the ETROC2 submission and has been used extensively for the preparation of the ETROC2 chip level testing as well as system level testing. In this presentation, the main ETROC2 design features along with the testing results will be summarized, followed by lessons learned from ETROC2 design, fabrication and testing experiences to guide the ETROC3 design.

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