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Development of FABulous: An Embedded FPGA Framework in 28nm CMOS

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FABulous is an open-source eFPGA framework developed by the University of Manchester, enabling programmable digital logic to be integrated into ASIC designs. In 2023, our team plans to submit a 28nm CMOS ASIC and explore flatten versus hierarchical design using HVT devices for radiation hardening. This 28nm eFPGA design will use SUGOI and PGPv4 to program and move data in and out of the eFPGA. Post-PnR simulation results will be presented, along with full chip co-simulation with firmware/software for pre-tape out validation results.

Summary (500 words)

With the push for future high energy physics detectors to move more processing to the edge in the effort to reduce data volumes at the earliest possible stage, the ability to use programmable digital logic further up the digital signal processing chain becomes more important. While embedded Field Programmable Gate Array (eFPGA) that is built into Application-Specific Integrated Circuit (ASIC) is nothing new, these frameworks were not free and were not open source. In recent years several popular FPGA architectures have become 20+ years old, which means that original patents have expired. In 2021 University of Manchester started a project called FABulous, which is an open-source eFPGA Framework.
FABulous has demonstrated eFPGA designs in 180nm CMOS and 130nm CMOS by the University of Manchester. In 2022 SLAC demonstrated an eFPGA design using FABulous in 130nm CMOS Multi-Process Wafer (MPW). For 2023 we plan to tape out a 28nm CMOS MPW in July 2023 and expect to receive the ASIC back in November 2023. The goal of using 28nm is to determine what programmable logic area density can be achieved while using HVT devices for radiation hardening.
This 28nm eFPGA design will use SLAC Ultimate Gateway Operational Interface (SUGOI), which is a lightweight 8B10B based serial protocol for register access, to load the eFPGA bitstream. Pretty Good Protocol Version 4 (PGPv4), which is a 64B66B based serial protocol design for Trigger Data AcQuisition (TDAQ) systems, will be used to move data in and out of the eFPGA.
Our team is exploring the use of flatten versus hierarchical design in the same digital ASIC tape out and will compare the programmable logic area density results before ASIC tape out. Since we will receive the ASIC design after this conference, we plan to present the results of the physical implementation and any post Place and Route (PnR) simulations at proceedings. Finally, we will discuss the full chip co-simulation with firmware/software for pre-tape out validation prior to the tape-out.

Author: RUCKMAN, Larry Lou Jr (SLAC National Accelerator Laboratory (US))

Co-authors: KIM, Hyunjoon (SLAC National Accelerator Laboratory (US)); ROTA, Lorenzo; GUPTA, aseemg

Presenter: RUCKMAN, Larry Lou Jr (SLAC National Accelerator Laboratory (US))

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