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The optimization, design and performance of the FBCM23 ASIC for the upgraded CMS beam monitoring system

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We present the development of the FBCM23 ASIC designed for the Phase-II upgrade of the Fast Beam Condition Monitoring (FBCM) system built at the CMS experiment. The FBCM system should provide reliable luminosity measurement with 1ns time resolution enabling the detection of beam-induced background. The FBCM23 ASIC comprises six channels of fast preamplifier working in transimpedance configuration followed with CR-RC3 shaper and leading edge discriminator. The paper will show the optimization of the design, overall architecture and the detailed implementation in a CMOS 65nm process as well as preliminary electrical performance.

Summary (500 words)

The primary role of the FBCM system is accurate luminosity measurement with 1ns time resolution that will provide the detection of beam-induced background. To meet this requirement from the physics point of view, the FBCM sensors should have a certain area and distance to the beam line, balancing occupancy, and acceptance. A good compromise between the area and position of the sensor is provided by 1.7×1.7mm silicon pad installed at a radius around 14.5cm. The radiation environment in this position is rather harsh, and the detector modules should stand up to 200Mrad of TID and particle fluxes up to 2.5×10ˆ15 N/cmˆ2 1MeV equivalent. Although the 65nm CMOS process can stand the expected TID dose without major issues, the increase of the leakage and degradation of charge collection efficiency (CCE) from the heavily irradiated sensors have to be taken into account during the noise optimization of the front-end amplifier and final choice of the sensor thickness. In order to provide a reasonable signal-to-noise ratio (SNR) above 10 at the end of the detector lifetime for any sensor option, the series noise contribution from the input transistor should be kept below 700e- ENC. Figure ENC3D6pF8.pdf shows the optimization of the input transistor dimensions and the bias for the worst case of 6pF input capacitance (e.g. 120□m sensor plus the parasitics).
The schematic of the preamplifier stage is shown in FBCMpreampTWP.pdf file. The input stage is built with the regulated telescopic cascode amplifier, with the NMOS input transistor of 2000/0.2 □m biased with 2.1mA and loaded with low voltage cascode PMOS sources. The simulated open loop gain and GBP is around 69dB and 3.5GHz respectively. The preamplifier works in transimpedance configuration with selectable feedback resistor (25 or 50kOhm). The block diagram of the full channel is shown in FBCMchanTWP.pdf file. The transimpedance preamplifier is DC coupled to the booster amplifier and leading edge discriminator. Although this intrinsically provides good stability of the baseline in case of high and variable hit rates, it is a less satisfactory solution from the standpoint of the mismatch variation which is amplified by DC-coupled stages. The DC variation at the discriminator input is nearly 100mV pk-pk and to compensate for this, two 8-bit threshold DAC's per channel have been employed. Another 8-bit DAC, common for the chip, is used for the global offset setting. The final gain of the full chain is around 60mV/fC. The adjustable RC filter provides adjustment of the peaking time between 6 and 8ns what helps in the optimization of SNR for various input load conditions. The outputs of the discriminators are sent outside the chip through SLVS interfaces. The ASIC comprises an internal calibration circuitry allowing for in-situ characterization of the chip. All bias and configuration registers are accessible via standard I2C interface. The FBCM23 ASIC has area of 3×3mmˆ2. The

chip has been submitted for MPW in May and the preliminary results from the electrical characterization are expected at the time of the workshop.

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