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Two HVCMOS active pixel ASIC designs for the Measuring GCR and SEP with a combined dynamic range of >80dB

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The design of HVCMOS pixel detectors for measuring Galactic Cosmic Rays (GCR) and Solar Energetic Particles (SEP) in space is presented. The design goals are: (a) cover a very wide dynamic range (from ~0.5fC to pC) and (b) minimize the power consumption. Two pixel designs were implemented, one tailored to the measurement of high energy depositions due to impinging ions and one with high gain for the low energy depositions resulting from minimum ionizing particles. Both designs have been fabricated in the LFoundry 0.15μm technology. The design choices are backed by simulation results and preliminary measurements.

Summary (500 words)

Fully depleted Si monolithic active pixel sensors (called HVCMOS or DMAPS) have been studied and introduced in high energy physics experiments for measuring minimum ionizing particles. However, for measuring GRC and SEP events in space, the sensor should be able to process charges with a dynamic range >80dB. Additionally, the specification for power consumption should be as low as possible. With these requirements in mind, we mean to respond to the demand for miniaturized instruments which could increase the crew autonomy for operational decisions related to radiation hazards and to the science opportunities resulting from the boost of planetary exploration.

To efficiently process the charge dynamic range, two sensor designs, one 'low gain'and one 'high gain'were implemented. Fig. 1. shows the block diagrams of the two pixels.

The low gain pixel does not contain a charge amplifier. The sensor cathode is held at the reset voltage due to the negative feedback of a buffer which also provides the path of the sensor's leakage current. When a particle traverses the sensor, the negative transition of the cathode voltage forces a comparator to quickly flip and disconnect the in-pixel sampling capacitor from the reset voltage and connect it to the sensor cathode instead. The capacitor voltage is proportional to the charge collected and is transferred to the array periphery to be digitized by a successive approximation ADC. Thus, a drastically reduced current consumption is achieved (35nA/pixel when idle).

For the high gain pixel, a diode connected NMOS is used to bias the sensing diode. The sensing diode capacitance required in this case should be of the order of 500fF for a 100 μm pitch pixel. A charge sensitive amplifier integrates the input charge signal on a 40fF feedback capacitor, along with a current source feedback for discharging. The CSA is decoupled for the sensor leakage path with capacitor CC. The subsequent ac coupled comparator produces the time over threshold pulse whose duration is not measured digitally in the pixel. Instead, it drives a time to voltage converter, whose output is transferred to the array periphery and digitized in the same way as the low gain version. The high gain pixel power consumption is approximately 8uA when idle, with the option of increasing/decreasing this number according to requirements.

The arrays designed and fabricated are 16 x 16 for the low gain and 32 x 32 for the high gain. The low gain array consists of pixels with dimensions 200 x 200 μm2 and it can process signals in the range from 40 fC to 9 pC. The high gain array has pixels with 100 μm pitch and it can process signals from 0.5 fC up to 50 fC. The gains of the two pixels are shown as a function of the dynamic range in Fig. 2.

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