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A Charge-integration Pixel Detector Readout Chip Features High Frame Rate with in-pixel ADCs.

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HYLITE (High dYmamic range free electron Laser Imaging deTEctor) is a charge-integration pixel detector readout chip designed for SHINE (Shanghai high repetition rate XFEL and extreme light facility). The chip features a frame rate of 10kHz and a successive readout mode. HYLITE200S is the third prototype chip in the HYLITE series, including correlated double sampling circuits to improve noise performances. The signal-to-noise ratio of the chip with a single 12keV photon injection is 9.31. To achieve high-speed data output, HYLITE200S incorporated a clock management block. Tests demonstrated that the data transmission can be achieved steadily at a speed of 3.125Gbit/s.

Summary (500 words)

The charge-integration readout chips of pixel detectors have been widely adopted in XFEL (X-ray Free Electron Laser) facilities. Almost all of them are designed for a specific light source according to the beam feature. SHINE is been built in Shanghai, China. The beam generated by SHINE will be successive pulses with a repetition frequency of 1MHz. Thus, the pixel detectors of SHINE must work in a successive mode to keep in sync with the beam. HYLITE is the pixel readout chip designed for SHINE with a frame rate of 10kHz and an automatic gain-switching function. To achieve such a high-speed readout in a successive mode, an ADC is integrated in each pixel so that the outputs of pixels are digital signals.

HYLITE200S is the third prototype chip in the HYLITE series with a pixel pitch of 200 μm. Prior to HYLITE200S, HYLITE0.1 and HYLITE0.2 were both manufactured using a 130 nm CMOS process and underwent full testing. The result showed that the in-pixel ADC scheme is successful. However, some issues were not been solved by these two tape-outs. For example, the signal-to-noise ratio of the original pixel is 2.31, which cannot fulfill the requirement of a single photon resolution of 12 keV. To improve the noise performance, a CDS (Correlated Double Sampling) circuit was added to the HYLITE200S pixel to mitigate the reset noise. The signal-to-noise ratio on the high gain stage of HYLITE200F is 9.31.

The I/O pads of a pixel readout chip are limited due to the single-side I/O structure. However, the amount of control signals in a HYLITE chip is large as many switch-capacitor circuits are adopted. A frame logic was designed to generate ten control signals according to two external signals: a clock and a frame refresh signal. Timing of the generated signals can be configured by a common SPI bus.

The array size of the full-size chip will be 128×128, resulting in a data rate of 3.28Gbit/s per single chip. In the full-size chip architecture, two high-speed serializers and corresponding CML (Current Logic Logic) drivers will be adopted. To validate the design, a clock management block and a high-speed data port were integrated into the periphery of HYLITE200S. The clock management block consists of a PLL (Phase Lock Loop) and a frequency divider. The high-speed data port includes an 8b10b encoding logic, a serializer, and a differential CML driver. An eye diagram analysis confirmed that the data port operates effectively at a data rate of 2 Gbit/s. By FPGA decoding, the data rate was further proved at 3.125 Gbit/s. These results demonstrate the successful design of the clock management block and the data port. In the next step, a full-size chip of HYLITE will be produced on the basis of HYLITE200S.

Primary author: LI, Mujin (IHEP)

Co-authors: ZHANG, Jie (Institute of High Energy Physics(IHEP), Chinese Academy of Sciences(CAS)); WEI, Wei

Presenter: LI, Mujin (IHEP)

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