MightyPix at the LHCb Mighty Tracker

Verification of an HV-CMOS pixel chip's digital readout

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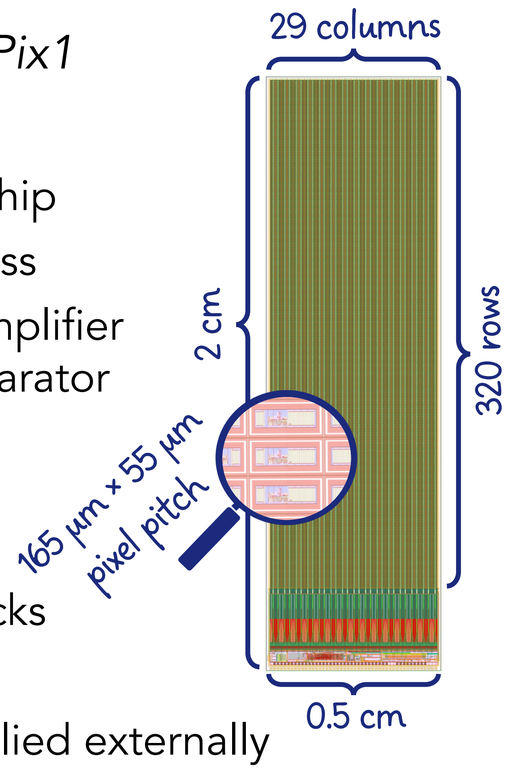
The Project | *LHCb Mighty Tracker*

- Hybrid tracker proposed for HiLumi LHCb [1]
- Mighty Tracker = SciFi + Silicon tracker
- Inner parts: HV-CMOS pixel chips [2] for radiation hardness and good granularity

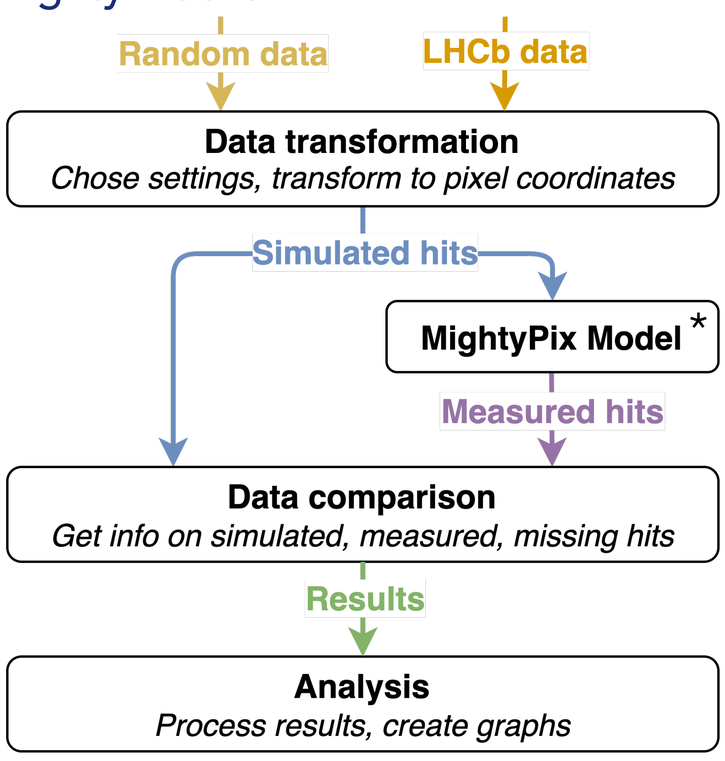
The Chip | *MightyPix1*

- First prototype
- HV-CMOS pixel chip
- TSI 180 nm process
- In-pixel CMOS amplifier and CMOS comparator
- Digital interfaces: TFC, I2C, SR
- External 40 MHz and 640 MHz clocks
- Internal PLL
- Bias voltages applied externally or via integrated 10 bit VDACs



The Simulation | *Goal and Method*

Can MightyPix1 handle particle hit rates at the Mighty Tracker?

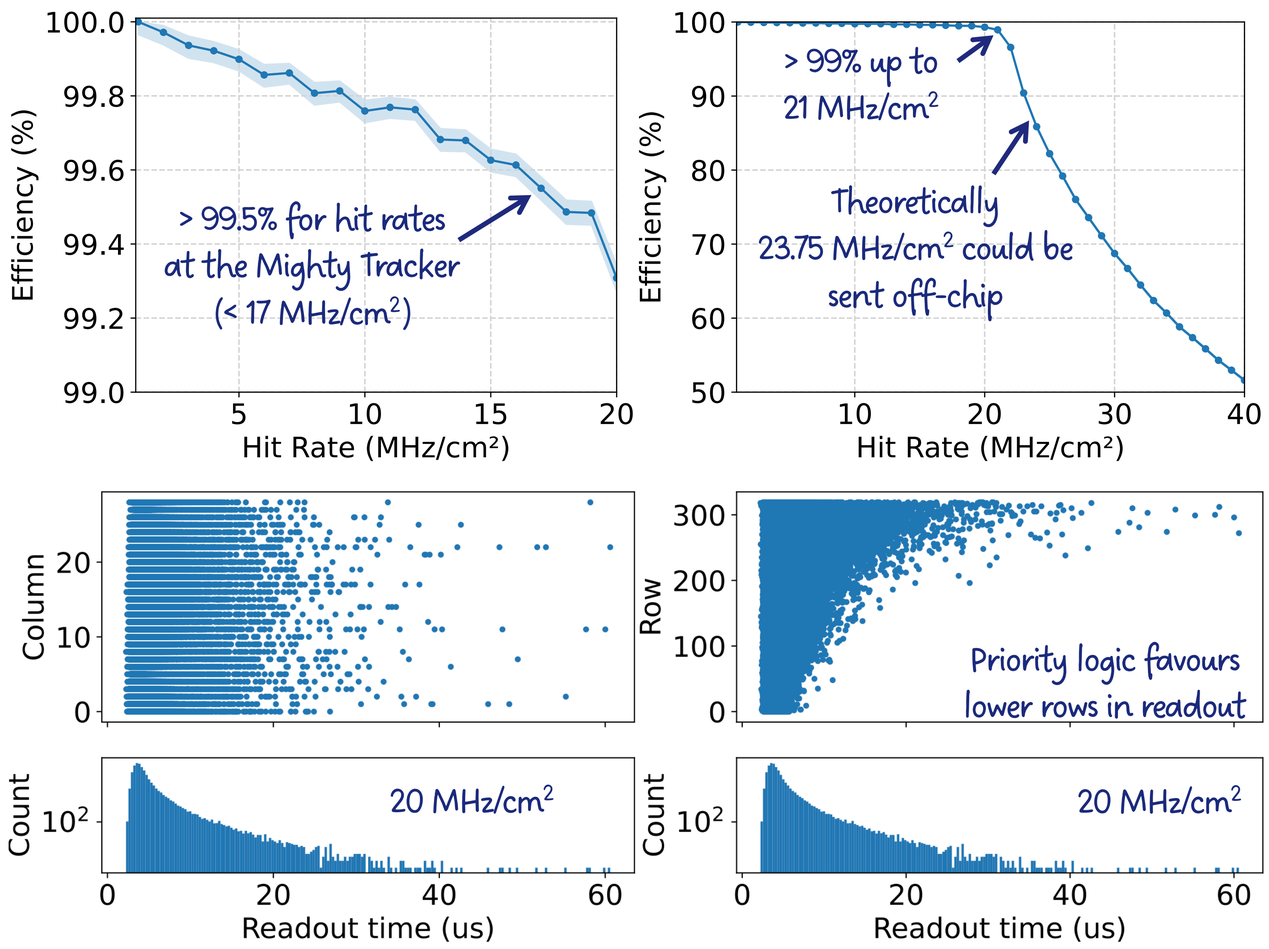


* Behavioural model, representing analogue pixel matrix with synthesised digital logic

[1] The LHCb Collaboration. Framework TDR for the LHCb Upgrade II - Opportunities in flavour physics, and beyond, in the HL-LHC era. CERN-LHCC-2021-012, LHCB-TDR-023, 2021.
*[2] I. Perić et al., High-Voltage CMOS Active Pixel Sensor, IEEE Journal of Solid-State Circuits **56** (2021) 2488.*

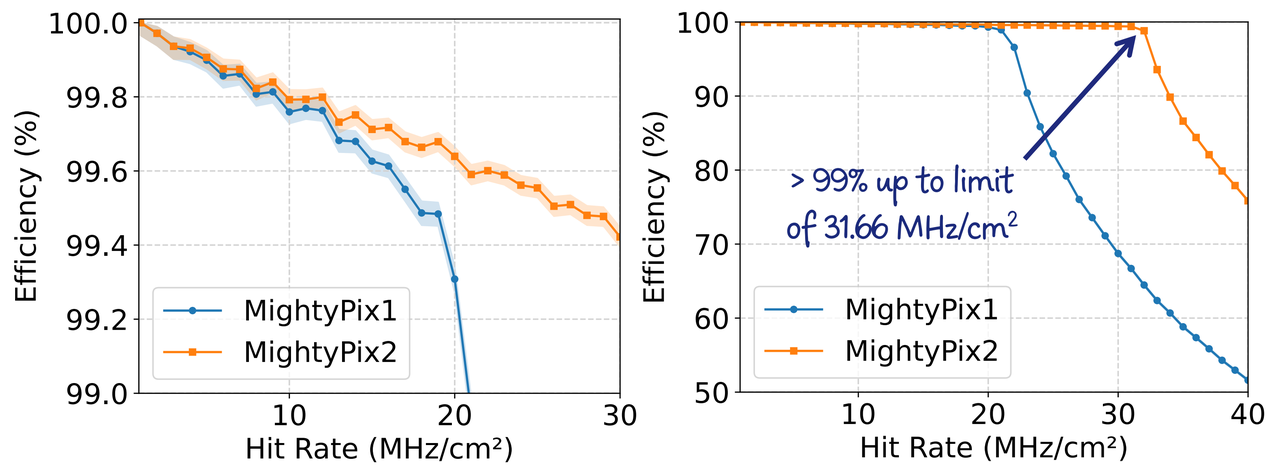
The Results | *Simulated MightyPix1 Efficiency*

- Data transmission ≤ 4 x 1.28 Gbit/s per chip
- Data size = 2 x 32 bits per hit
- Max hit rate that can be sent off-chip = 23.75 MHz/cm^2
- Simulated efficiency drops at 21 MHz/cm^2



The Results | *Improvements for MightyPix2*

- Additional FIFO to free up hit buffers faster
- Reduced data size: 1 x 48 bits per hit
- Max rate that can be sent off-chip = 31.66 MHz/cm^2
- Simulated efficiency only drops at readout limit of 31.66 MHz/cm^2



Conclusion | *MightyPix1 can handle Mighty Tracker rates*

- New HV-CMOS chip MightyPix under development for LHCb Mighty Tracker → Expect hit rates up to 17 MHz/cm^2
- Readout mechanism of MightyPix1 studied in simulations
- Simulated MightyPix1 efficiency over 99% for hits rates up to 20 MHz/cm^2
- Simulations with new readout mechanism for MightyPix2 show efficiency over 99% for hit rates up to 31 MHz/cm^2