Contribution ID: **64** Type: **Poster**

Design of a very low power 12 bits 40 MS/s ADC based on a time-interleaved SAR architecture

Tuesday 3 October 2023 15:00 (20 minutes)

The paper describes a new figure of merit reachable in term of very low power dissipation for a 12 bit, 40MS/s Analog to Digital Converter in a CMOS 65nm process with 1V power supply. A differential time interleaved successive approximations register architecture is used. Each individual ADC channel is optimized regarding power consumption hence parallelizing 28 ADC channels in an analog memory like method, the total power consumption is only 280µW including all the reference voltage drivers and the digital sections. The total layout area of this converter is 0.87 mm2. Crosstalk simulations results will be discussed regarding channel-to-channel discrepancies.

Summary (500 words)

In view of next generation of high granularity detectors, the necessary density for the readout systems leads to the design of various multichannel integrated circuits. 64 or 128-channel chips are becoming common. In the same time there is an increasing need to reduce the power dissipation. Since digitization stages are more and more integrated within the front-end circuit, low power and high resolution converters will play a key role in next generation read-out circuits. We introduce here one low power solution based on time interleaved SAR converters. Many publications pointed out that SAR ADC in 65n process or below becomes one of the best choice for power reduction. In the same time many laboratories has published in the past very aggressive design based on so called “analog memories ”which are array of sampled capacitors with or without input buffers. In the present design, we combine these two concepts to display a more aggressive feature in low power ADC.

Usually time interleaved ADC targets high-speed results (beyond GS/s). Nevertheless, our simulations results show that even around 40MS/s we can reach lower power dissipation compared to other Nyquist architectures (pipelined, fast SAR or even pipelined SAR). A fast sampling feature combined with a set of slower conversion stages, help finally to save power because the constraints on dynamic power is relaxed. In our design, each channel of ADC is coming with its own reference buffers. This helps to reduce significantly the crosstalk. The input sampling path includes bootstrap switches to compensate the linearity issues. We target in the present design 12 bits 40MS/s interleaving 28 ADC channels, each one converting at 1.5MS/s, based on a segmented array of capacitors. Due to the sensitivity of segmented architectures to mismatch and parasitic capacitors, we include an additional automated trimming algorithm to make the design robust against non-linearity and distortions issues. According to our simulations, the total power dissipated is only 280µW when sampling at an equivalent frequency of 40MS/s.

The layout of each elementary ADC channel occupy an area of 40µm*780µm. Hence, the total 28 interleaved ADC area is about 0.87mm2. The layout is organized to path the way for future multi-channels 40 MS/s ADCs.

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Session Classification: Tuesday posters session

Track Classification: ASIC