Time-Delay-Based Analog Front-End for Monitored Drift Tubes in 65 nm CMOS with < 200 ns Baseline Recovery Time and Coherent Time-over-Threshold

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Abstract. Monitored Drift Tube (MDT) chambers for muons detection at ATLAS Experiment adopt analog front-end read-out electronics for precise-tracking/momentum measurements of detected particles [1]. State-of-the-art has historically used bipolar shaping electronics (at approximately 800 ns baseline recovery time [2]) that scarcely fits with High-Luminosity (HL) requirements where small-MDT (sMDT [3]) are used at 180 ns input signal time-width. This brief presents 4-channels Application Specified Integrated Circuit in 65 nm CMOS for sMDT signal amplification and shaping that performs < 200 ns baseline recovery time and avoids distortion of Time-over-Threshold (ToT) characteristic due to multiple close input charge pulses composing sMDT signal.

Introduction. ATLAS (s)MDT charge-to-voltage conversion is performed by Charge-Sensitive-Preamplifier (CSP) feeding analog signal processing stages differentiated by Unipolar or Bipolar shaping circuits. Due to complex requirements of unipolar shaping circuits bipolar shaping schemes are preferred.
However, in classical readout electronics [2], Bipolar shaping circuits suffer from long Baseline Recovery Time (BLR), higher than 800 ns, unfit for >1 MHit/sec required by HL-sMDT experiments [3]. Another drawback with current readout electronics is that the secondary pulses due to main track superimpose the main pulse, hence ToT is not correlated to main pulse. These problems are even more critical in sMDT chamber which has drift-time of 180 ns. To profit from high date rate sMDT performance, BLR time must be less than the drift-time and ideally with no pile-up effects.

Method. The proposed ASIC is based on an innovative time-delay-based technique that significantly accelerates the BLR time performance. The qualitative block-scheme and time-domain evolution of the proposed approach are shown in Fig. 2. The incoming sMDT multiple charge signal is processed by <10 ns rising time CSP for charge-to-voltage conversion. Key performance parameters of CSP are fast peaking-time and noise performance which are optimized by using high input device transconductance (i.e. = 25 mA/V). CSP output feeds Low-Pass-Filter (LPF) whose differential input signal is composed by voltage difference between CSP output and a delayed replica. This way, along the rising time of the CSP output voltage, the LPF output signal maintains the fast shaping while along the decay phase accelerates the BLR time, removing some electrical power from CSP main pulse output signal.
Delay Stage is composed by simple phase-shift R-C network feeding a voltage buffer for driving LFP input impedance. This way, the LPF performs both single-to-differential and unipolar-to-bipolar conversion of the CSP output voltage signal. Accuracy of the phase shift is essential and for this reason the capacitor of the Delay Stage is designed by binary weighted 5-bit programable capacitor array to achieve a programable time delay. Finally, the resulting < 180 ns BLR time bipolar signal is fed into comparator which compares it with a programable threshold value to generate ToT signal. The complete electrical scheme of the integrated analog front-end is shown in Fig. 3,

Results. Design is validated by both ideal δ-Dirac input pulse (Fig. 4) and sMDT Garfield signal (Fig. 5-6) (swept in 5-100 fC range) by Post-Layout Extracted View (PEX) simulations.
Fig. 4 displays a peaking time of 13 ns with a sensitivity (Output voltage/Input charge) of 8 mv/fC. BLR time is reduced, by 78% as compared to classical models, to 165 ns that is even less than the drift time of sMDT chamber.
Fig. 4 shows channel transient response for δ -delta pulse. Garfield input signal is shown in Fig. 5 for which channel transient response is shown in Fig. 6 and ToT in Fig. 7. Fig. 8 shows the ToT range as input charge pulse varies from 5-100 fC. Secondary pulses crossing threshold value are suppressed by an asynchronous finite-state-machine logic triggered by falling-edge of ToT.

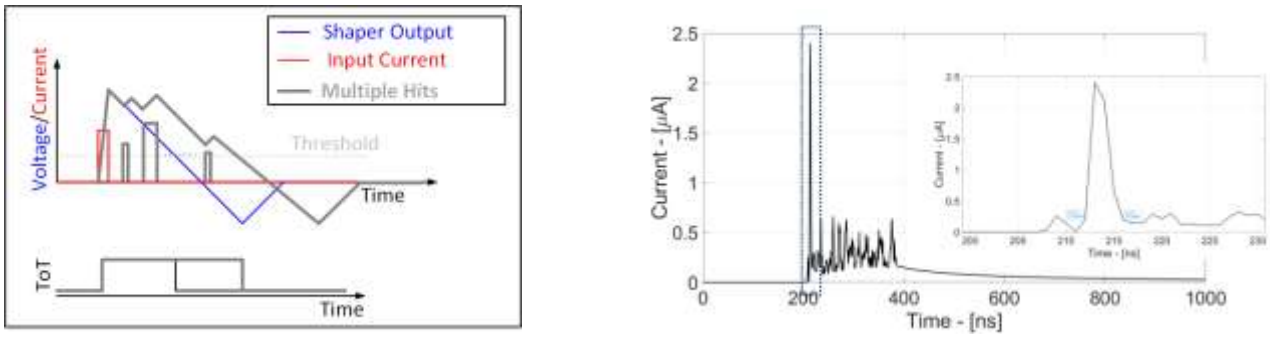

Fig. 1 – Qualitative (left-side) and Measured (Right-Side) small Monitored Drift Tube (sMDT) Output Charge

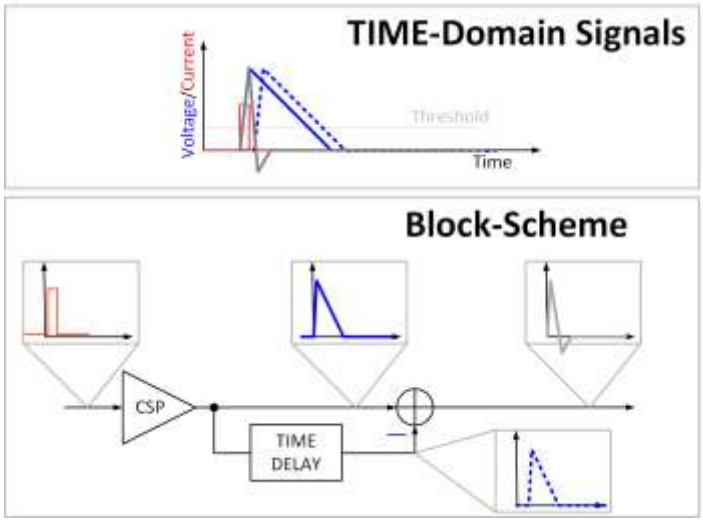

Fig. 2 – Block-Scheme of the Proposed Time-Delay-Based sMDT Signal Processing

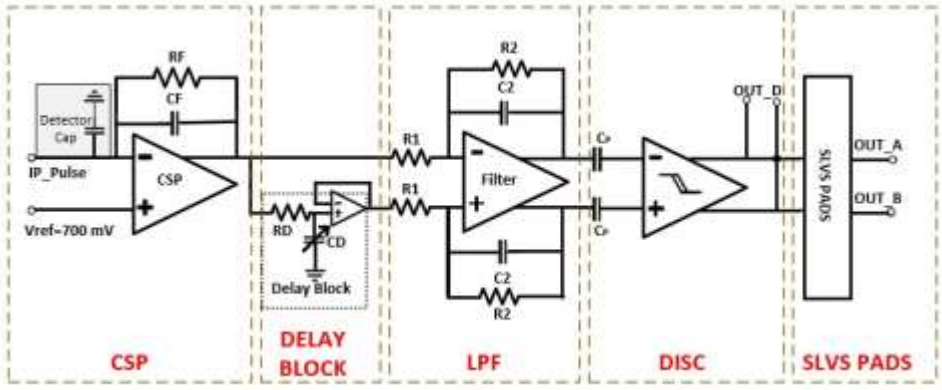

Fig. 3 – Single Channel Architecture of Readout Channel

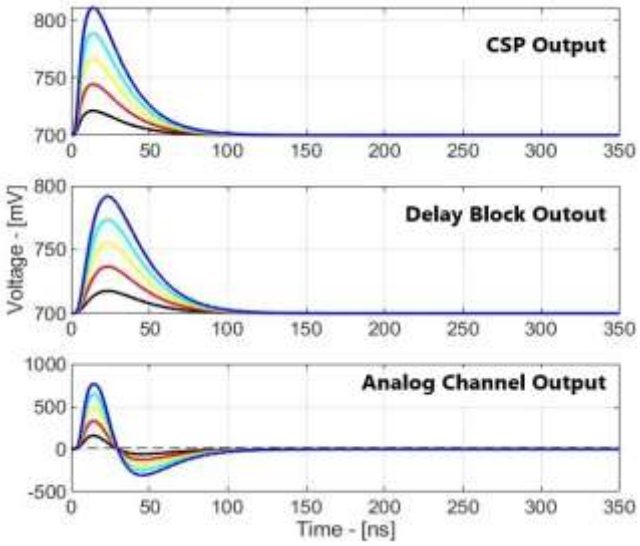

Fig. 4 – Transient Response of Analog Channel for 20 – 100 fC dirac-delta input pulses

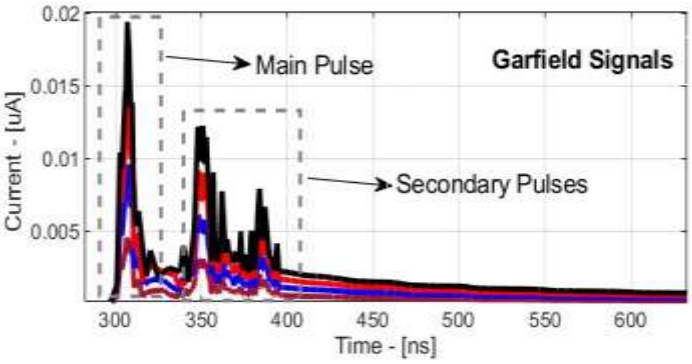

Fig. 5 – Garfield Input signal scaled from 20 – 100 fC main pulse

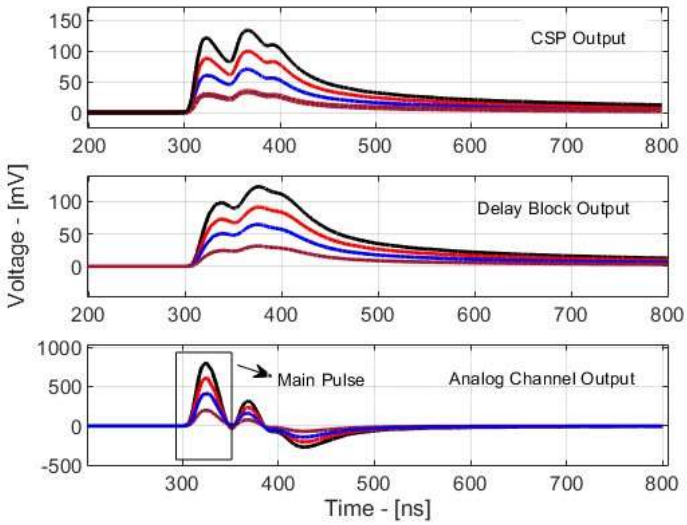

Fig. 6 – Transient Response of Analog Channel for 20 – 100 fC Garfield main pulses

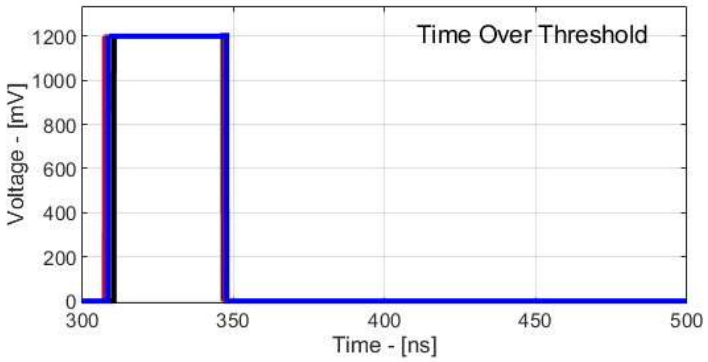

Fig. 7 – ToT due to Main input pulse for Input charge 20 - 100 fC

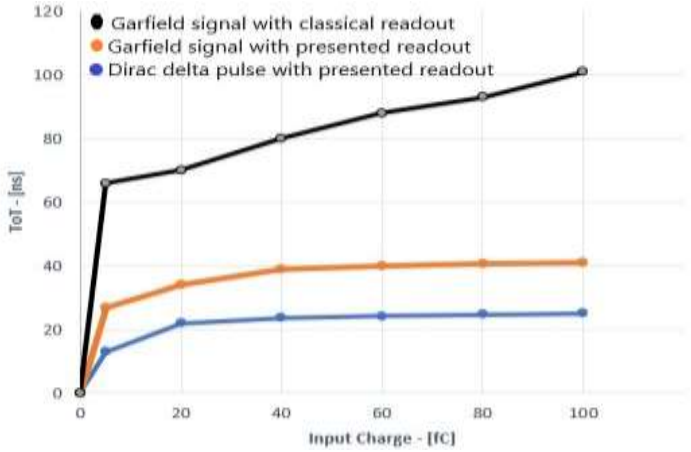

Fig. 8 – Time Over Threshold for 5-100 fC Input charge for presented and classical readout systems

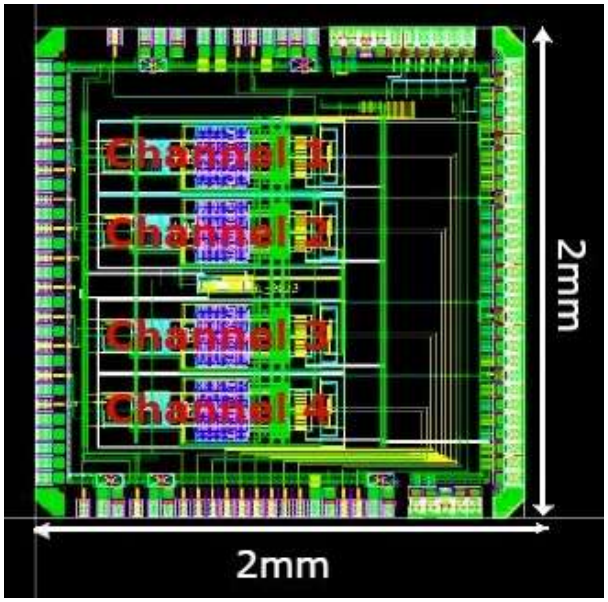

Fig. 9 – ASIC 4-Channel Layout Photo

References

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[3] O. Kortner et al; Schmidt-Sommerfeld, K.; Schwegler, P. Precision muon tracking detectors and read-out electronics for operation at very high background rates at future colliders. Nucl. Instrum. Methods Phys. Res. Sect. A Accel. Spectrometers Detect. Assoc. Equip. 824, 556–558, 2016