Figures

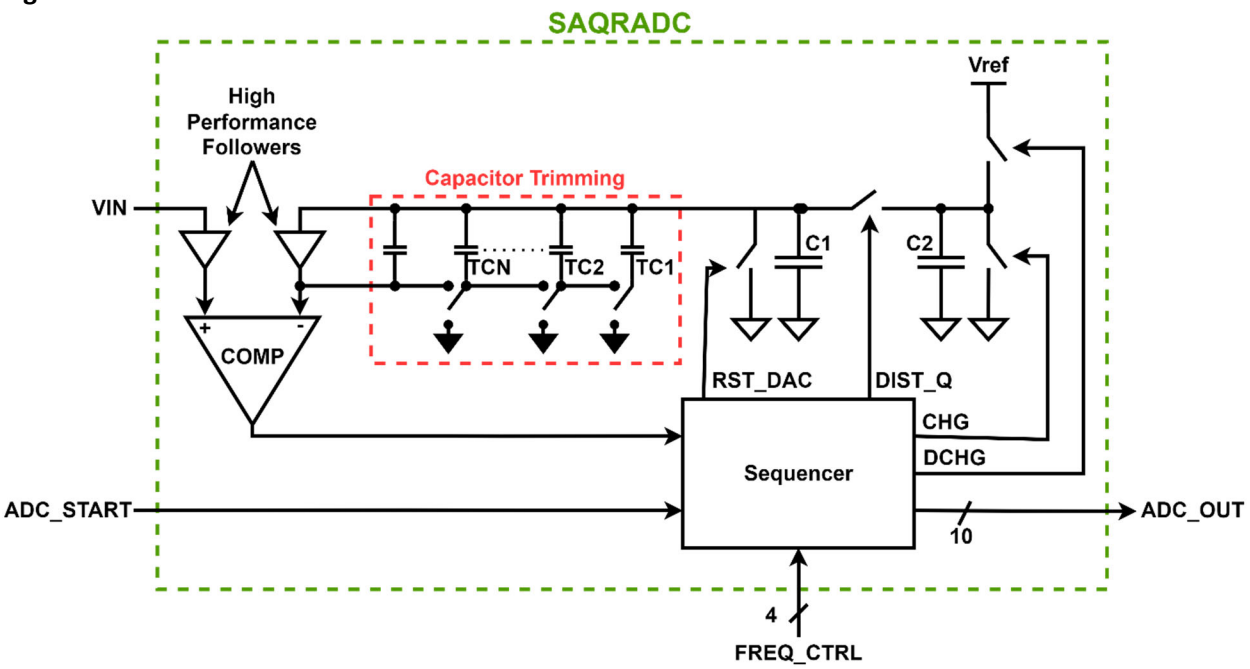

Figure 1: Top-Level Block Diagram of SAQRADC

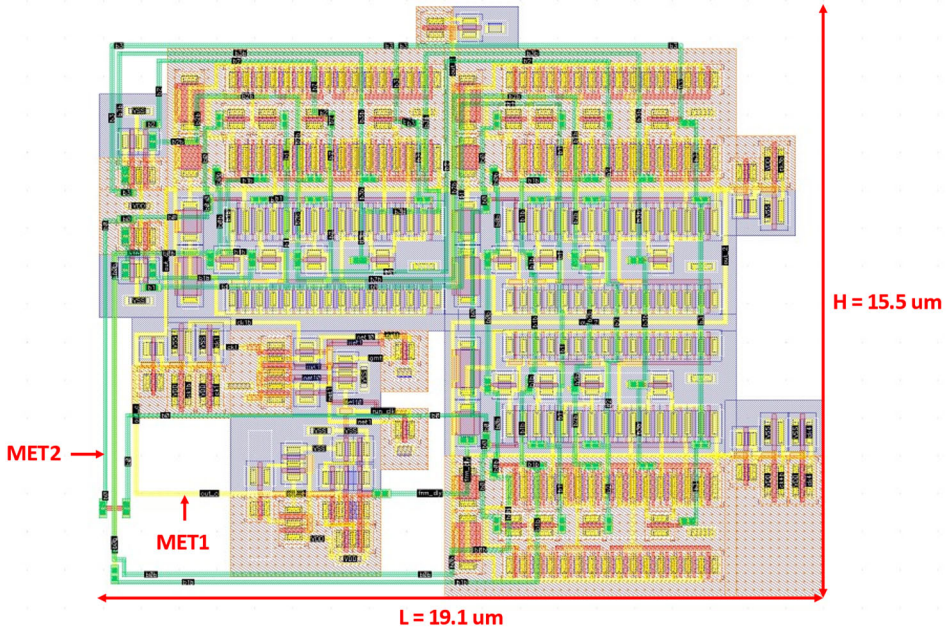

Figure 2: Example Layout of Clock Generator within Sequencer

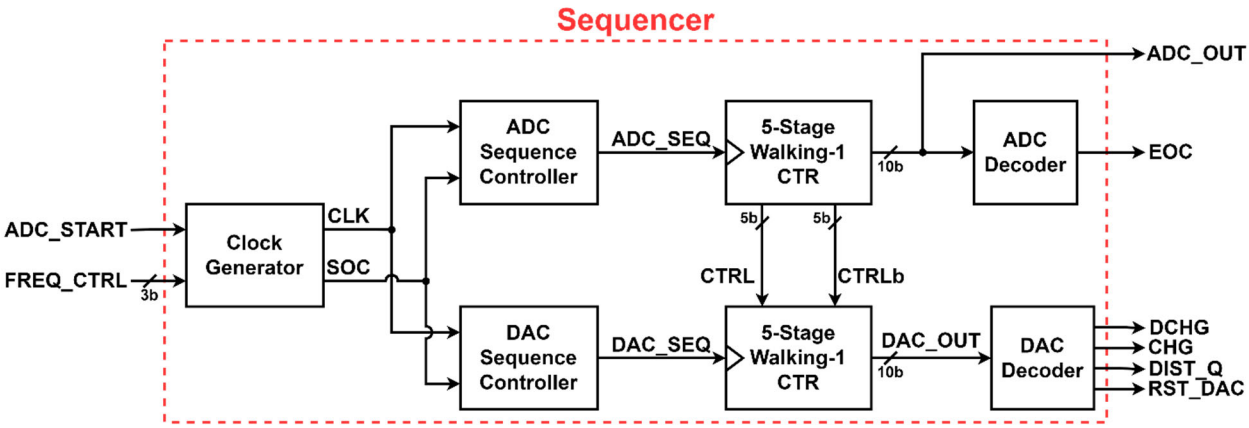

Figure 3: Sequencer Block Diagram

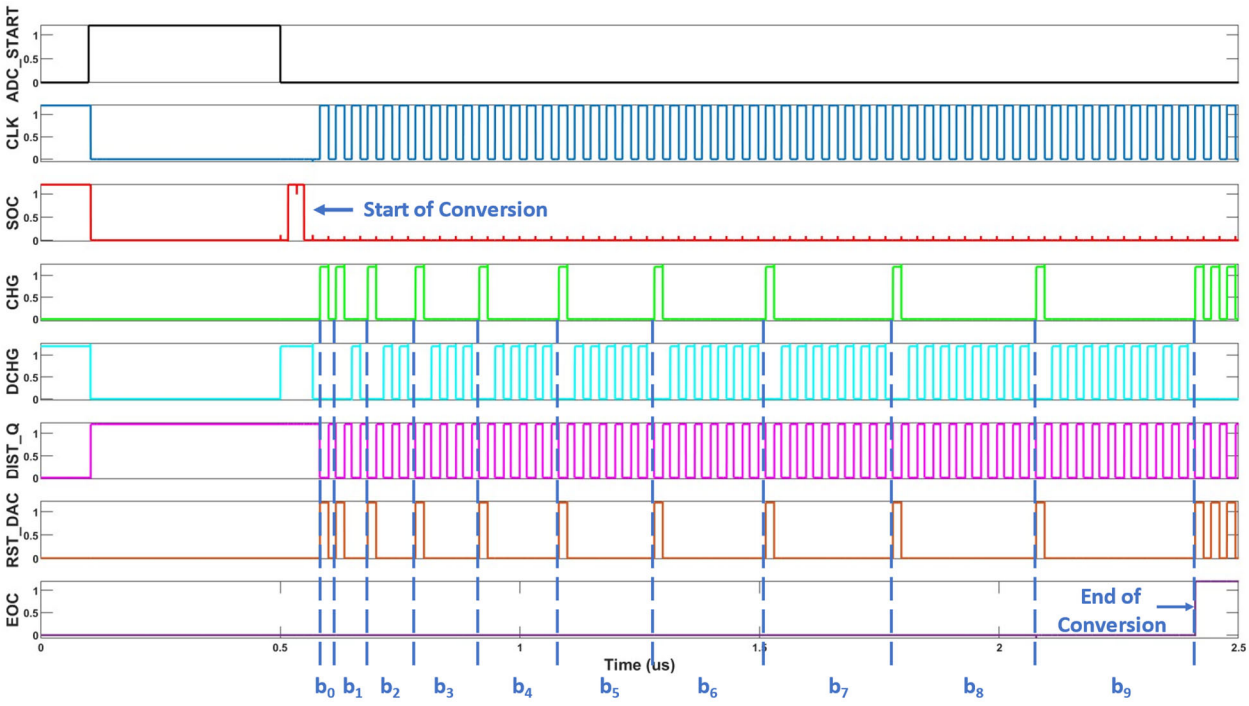

Figure 4: Sequencer Waveforms
(Waveforms Top to Bottom: ADC_START (Light Blue) | SOC (Green) | CLK (Purple) |CHG (Yelow) | DCHG (Red) | DIST_Q (Orange) | RST_DAC (White) | EOC (Pink))

Process	Input Range [V]	ENOB	Energy/Conversion [nJ]	Wake-Up Time [ns]	Layout Area [um^2]*
TPSCo 65 nm	0 – 1.2	9	0.212 – 2.02 (T_{CONV} = 0.82 -8.36 us)	22.6 – 218.6	~ 10,000

Table 1: ADC Characteristics (Based on Simulation)
**: Estimated*