Contribution ID: **200** Type: **Poster**

Design Updates for HPSoC: A very high Channel Density Waveform Digitizer with sub-10ps resolution

Tuesday 3 October 2023 15:00 (20 minutes)

We present the architectural design, prototype fabrication and and first results for the High Pitch digitizer System-on-Chip (HPSoC). The HPSoC is a high channel density and scalable waveform digitization ASIC with an embedded interface to advanced high-speed sensor arrays such as e.g. AC-LGADs. The chip is being fabricated in 65nm technology and targets the following features: picosecond-level timing resolution; 10 Gs/s waveform digitization rate to allow pulse shape discrimination; moderate data buffering (256 samples/chnl); autonomous chip triggering, readout control, calibration and storage virtualization; on-chip feature extraction and multi-channel data fusion.

Summary (500 words)

In recent years, the introduction of very fast optical sensors with extremely low pitches (e.g. Low Gain Avalanche detectors -LGADs) has enabled high-density designs for high energy and nuclear physics detectors offering excellent spatial and timing precision; the performance of detector systems composed of large arrays of such components is currently limited mostly by the readout capabilities of the existing readout electronics. To address these issues, we studied and designed the architecture of the HPSoC, a customized multi-channel waveform digitizing readout that is capable of directly interfacing with state-of-the-art sensor arrays, can extract relevant information from each pixel's interaction and internally combine such information in a compact digital format, with timing precision at the picoseconds level and capable of sub-pixel spatial precisions at a few tens of micrometers or less. The design has targeted the following specifications and features:
An input preamplification handling fast current-based sensors (~100 ps rise times);
A timing resolution of at least 5ps with a target of 1ps;
Very large integration (100+ channels) with modular tileable, scalable structure;
Waveform digitization of at least 10Gs/s, allowing for pulse shape discrimination;
Moderate data buffering (256 samples/channel);
Autonomous chip triggering and storage virtualization;
On-chip feature extraction and multi-channel data fusion;
In this presentation we concentrate on the features related to the digitization and data processing as the preamplification has been described elsewhere.

The architectural design of the HPSoC was performed based on the following ideas:
A dense sensor array has all its outputs connected directly to the input of the HPSoC. The connection is performed through bump bonding to area IOs on the asic:
The HPSoC is modularly built as an equivalent array of "tiles", each fully capable of independently gathering data from the corresponding pixel.
The signal is initially going through an analog conditioning stage composed of a transimpedance amplifier to convert the current input into the proper input voltage range for the subsequent processing
A mixed signal section performs then a continuous waveform sampling while a trigger (external or generated by a local discriminator) selects a subset of samples for digitization.
The digitized data is then transferred to a digital component that performs on the fly amplitude and timing calibration, and extracts timing and amplitude (charge) information.
The time and charge information is finally transferred to a data concentrator that can optionally perform data

fusion to provide an accurate estimation of the arrival position with a sub-pixel accuracy, and a sub-sampling time estimate of the event arrival.
In order to demonstrate the feasibility of the design and test some of its critical components, a prototype chip containing most of the parts and with 4 fully functional channels was fabricated. The digital front end and back ends have also been designed for future integration. The chip is currently under evaluation and we will report the results of the first measurements. Upon satisfactory test completion, we will proceed designing, fabricating and testing a fully functional revision incorporating front end and back end digital partitions.

Primary author: MACCHIARULO, Luca

Co-authors: CHOCK, Chris (Nalu Scientific, LLC); UEHARA, Greg; Dr MOSTAFANEZHAD, Isar (Nalu Scientific, LLC)

Presenter: Dr MOSTAFANEZHAD, Isar (Nalu Scientific, LLC)

Session Classification: Tuesday posters session

Track Classification: ASIC