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The Analog Front End for FastRICH: an ASIC for the LHCb RICH Detector Upgrade

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This work presents the analog circuitry of the FastRICH ASIC, a 16-channel ASIC, developed in a 65 nm CMOS technology specifically designed for the RICH detector at LHCb to readout a wide range of detectors like Photomultiplier Tubes, to be used at the LHC Run 4 or SiPMs, candidates for Run 5. The front-end (FE) stage has an input impedance (Zin) below 50 Ω and an input dynamic range from 5 μA to 5 mA with a power consumption of ˜5 mW/channel. The chip includes a Constant Fraction Discriminator (CFD) and a Time-to-Digital Converter (TDC) for digitization.

Summary (500 words)

The increase in luminosity during HL-LHC Run 5 causes a challenging rise in particle multiplicity and hit occupancy also for the RICH subsystem. The increased irradiation level dictates a shift in the electronics from FPGAs to a more radiation-hard ASIC with a time resolution of better than 100 ps in order to keep the high particle ID performance after the Upgrade II. The FastRICH ASIC is under development in a 65 nm CMOS technology specifically designed for the RICH detector at the LHCb experiment. It builds on the experience with the FastIC ASIC and adds specific characteristics required for the RICH detector such as: (1) a Constant Fraction Discriminator (CFD) to minimize time walk variations and avoid the need to send the time-over-threshold information to correct for pile-up, reducing the amount of output data; (2) a Time-to-Digital Converter (TDC) to digitize the data; (3) a digital zero suppressed readout circuit; and (4) programmable output links for data transmission. The chip is radiation tolerant by design and the power consumption per channel is ˜5 mW.

This work presents the analog circuitry of the FastRICH ASIC. The Front-End (FE) stage processes the input signal in current mode with an input impedance (Zin) below 50 Ω and an input dynamic range from 5 μA to 5 mA. It is programmable to work with positive or negative input polarity signals delivered by low capacitance sensors with intrinsic amplification, such as Photomultiplier Tubes (PMT), small area (1x1 mm2) Silicon Photomultipliers (SiPM), or Microchannel Plates (MCP). Thus, this ASIC is suitable for the readout of MAPMTs in LHC Run 4 and the candidate SiPMs during Run 5. The FE consists of two complementary (positive and negative polarity) input stages based on a high performance unity gain current mirror with two control feedbacks. The Low Frequency Feedback (LFF) adjusts the input DC voltage with a range of adjustment of ˜400 mV to compensate for SiPM gain variations locally. A DC Level Shifter allows a larger input voltage adjustment range. The High Frequency Feedback (HFF) maintains Zin low at high frequencies. The most susceptible analog blocks are designed with Enclosed Layout Transistors (ELT) to improve its radiation tolerance.

Time-of-Arrival measurement is generated through a CFD. In addition, the ASIC will also provide a nonlinear Time Over Threshold (ToT) energy signal through a Leading-Edge Discriminator (LED) for calibration purposes. Simulations results regarding time walk are <150 ps for the CFD and <1.6 ns for the LED. CFD (and LED, optionally) binary output signal will be digitized on-chip by means of a TDC with adjustable time bin, ˜25 ps for the high-performance mode or ˜50 ps for the low-power mode. The digital circuitry will be implemented using Triple Modular Redundancy (TMR) to improve radiation tolerance.

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