Prototype of a 10.24Gbps Data Serializer and Wireline Transmitter for the readout of the ALICE ITS3 detector

on behalf of the ALICE collaboration

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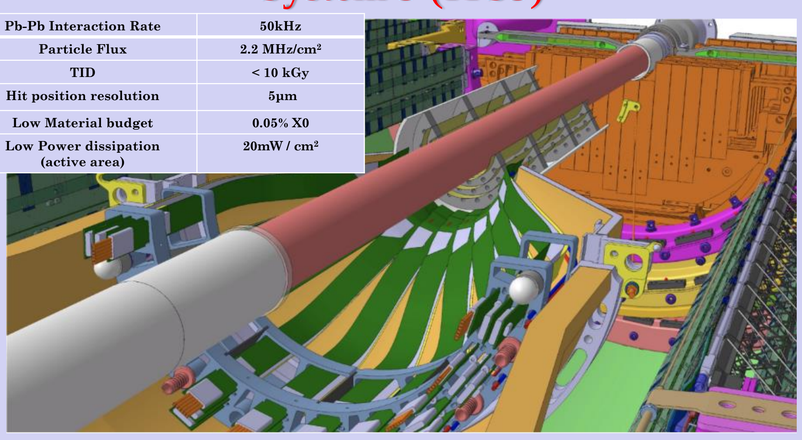
Abstract

A new silicon tracker detector (ITS3) will be installed in ALICE Inner Tracking System during the LHC long shutdown 3. We develop a 10.24Gbps Data Serializer and Wireline Transmitter (GWT-PSI) circuit for the readout of the detector. The Serializer circuit is based on a Multiplexer + DLL architecture which allows to achieve low power consumption (28mW) and to avoid high-frequency (> 640MHz) clock signals to be used. A clock-cleaning PLL and a power-supply cleaning LDO will be built into the GWT-PSI circuit making it immune to the noisy operation environment. Two test chips with the prototypes of the separate building blocks (Serializer + Line Driver, PLL, LDO) have been submitted in the ER1 production run in the TPSCo 65nm ISC CMOS imaging technology.

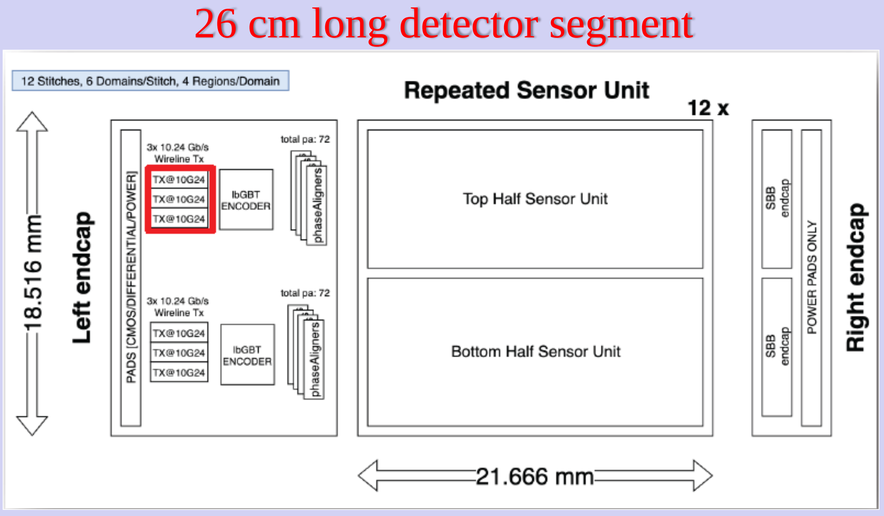
Vertex Detector in ALICE Inner Tracking System 3 (ITS3)

Pb-Pb Interaction Rate	50kHz
Particle Flux	2.2 MHz/cm²
TID	< 10 kGy
Hit position resolution	5μm
Low Material budget	0.05% X0
Low Power dissipation (active area)	20mW / cm²



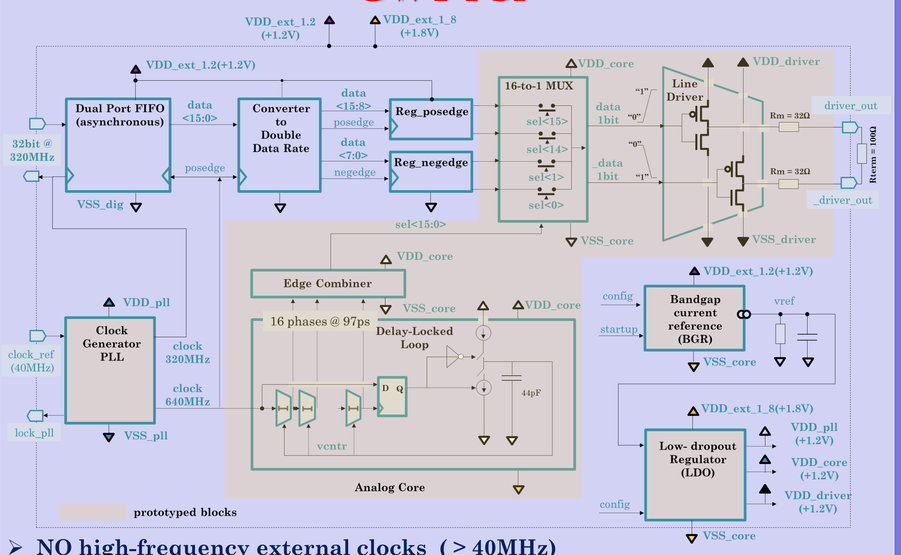
- Vertex detector in 65nm MAPS technology (pixel size ~20μm)
- 3 curved single-die detector layers (radius 18/24/30 mm)
- each sensor die is a 28cm long (wafer-scale) ASIC chip thinned to 50μm

26 cm long detector segment



- 6 high-speed (~10Gbps) data transmission links per chip required

GWT-PSI

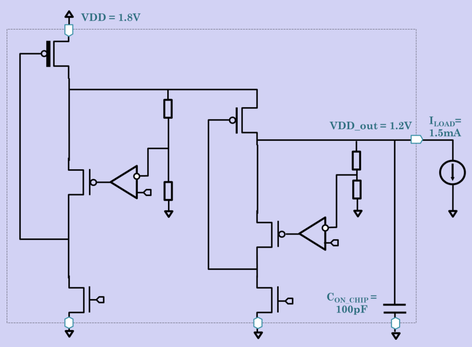


- NO high-frequency external clocks (≥ 40MHz)
- clock-cleaning PLL (ring-oscillator) : internal jitter < 6ps rms
- built-in power- supply- cleaning LDO
- voltage-mode transmitter (line driver): output swing = ±0.6V @ Rterm=100Ω
- low power : 28mW

Power supply voltage-cleaning LDO regulator

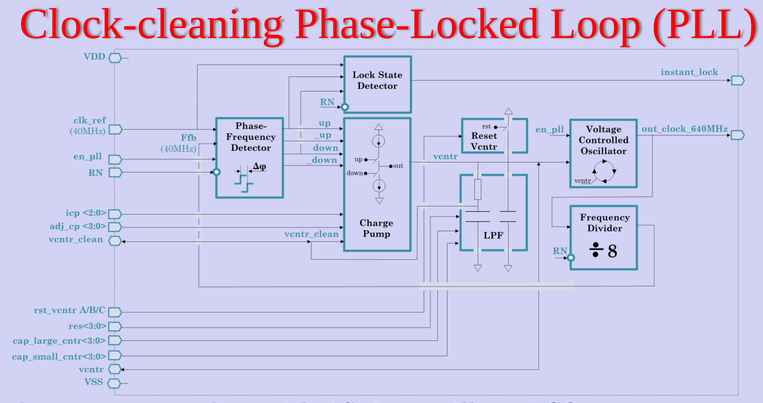
a 2-stage output-capacitorless LDO circuit

VDD	1.8V
Vout	1.2V
ΔVout / ΔVDD	-50dB @ <1MHz -32dB @ 110MHz (worst case)
Iload	1.5mA
ΔVout / ΔIload	1Ω @ DC 15Ω @ 100MHz (worst case)
Power consumption (internal)	0.74mA = 1.8V × 0.41mA



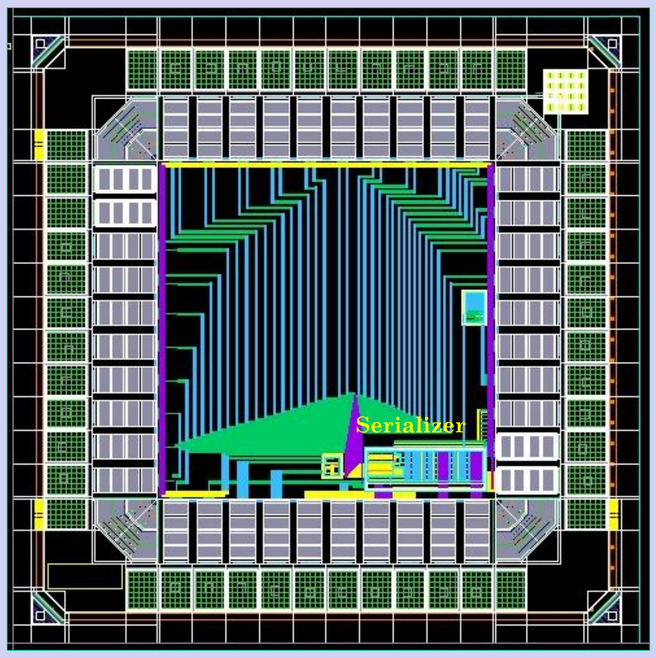
- suppresses expected (a 100mV p-p) power supply noise down to a 3mV level

Clock-cleaning Phase-Locked Loop (PLL)

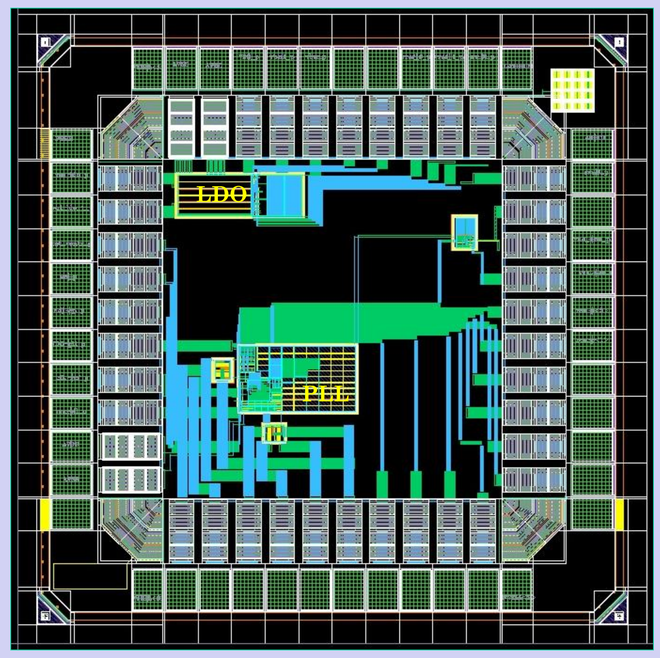


- charge pump topology with RC ring-oscillator VCO
- generates a low-time-jitter (rms 6ps) clock signal (640MHz)

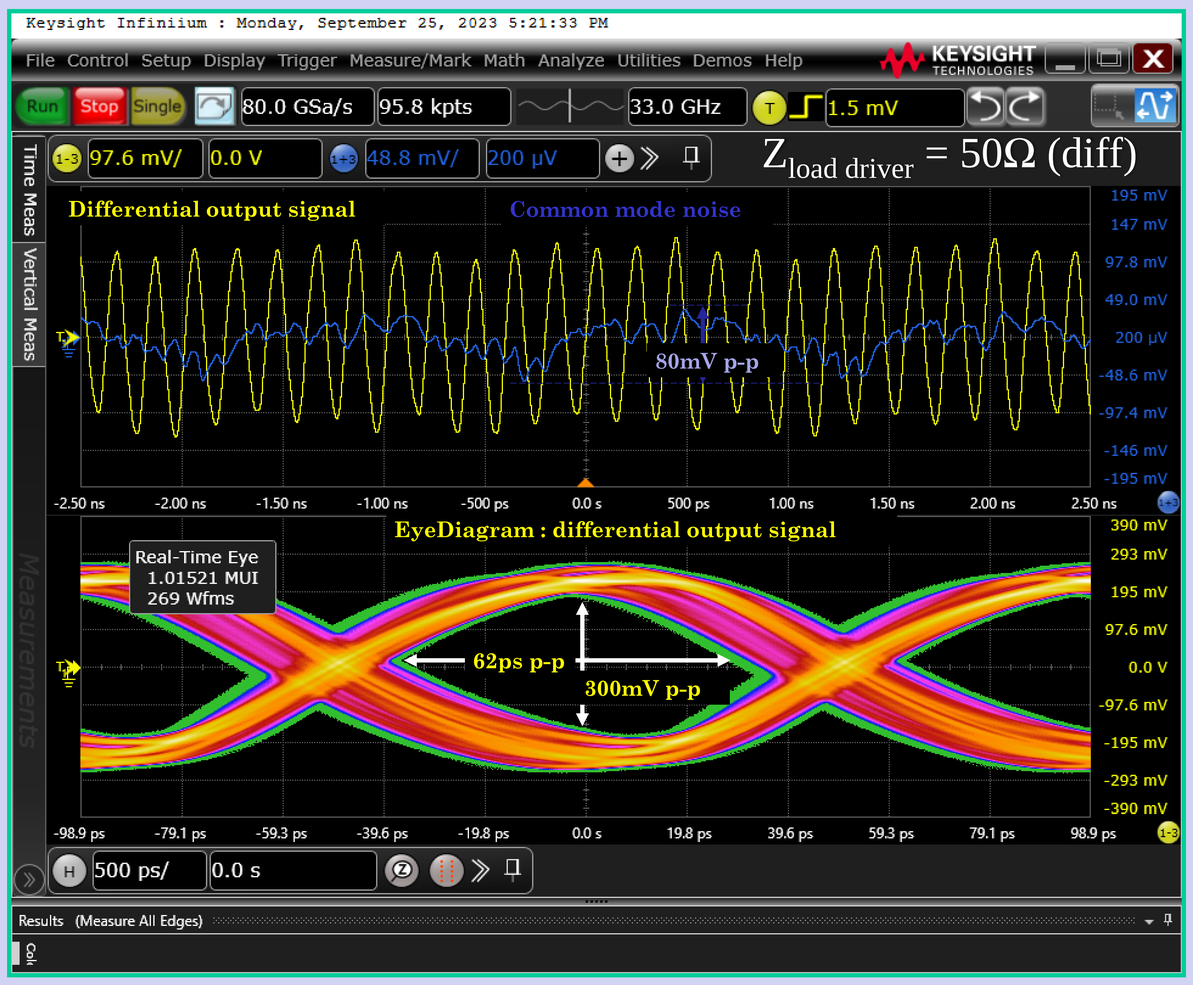
Prototype of the Serializer + Line Driver circuit (NKF7 test chip)



Prototype of the LDO and the PLL circuits (NKF6 test chip)



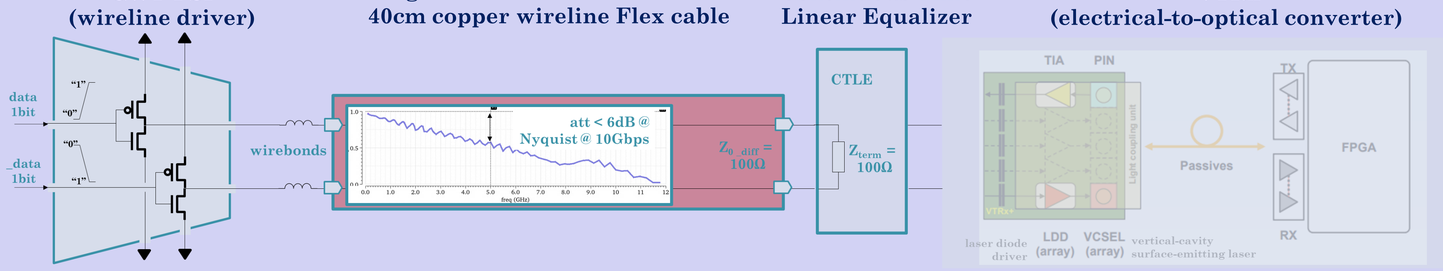
Measurements of the Serializer prototype @ 10.24Gbps, data pattern: 01010101



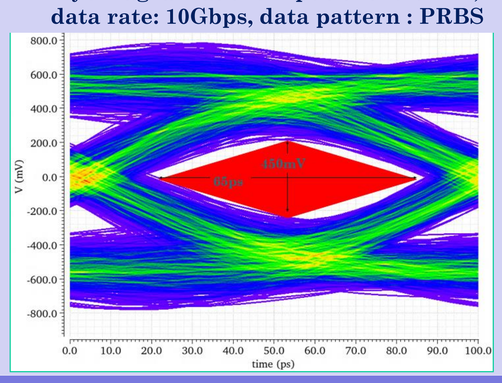
- the performance of the DLL (mismatch of the phase-to-phase intervals) as well as the performance of the Multiplexer and the Line Driver is usually characterized by the measurements when a clock-like data pattern (01010101) is applied to the input of the Serializer. In this case the inter-symbol interference (ISI) outside the chip has no effect as in the case of the PRBS data pattern
- the measurements show sufficient eye opening : width=62ps p-p, height = 300mV p-p @ a 50Ω differential load at the Line Driver (a 100Ω resistor on the test board in parallel with two ac-coupled 50Ω inputs of the scope)
- the cause of the common mode distortion (80mV p-p) is to be found

Evaluation (simulations) of the data signal transmission link

GWT-PSI (wireline driver) | Signal transmission channel : 40cm copper wireline Flex cable | Continuous Time Linear Equalizer | VTRx (electrical-to-optical converter)



EyeDiagram at the input of the VTRx, data rate: 10Gbps, data pattern : PRBS



- the inter-symbol interference (ISI) caused by the limited bandwidth of the transmission channel (Flex cable, chip wirebonds, on-board connectors, etc) will deteriorate the shape of the signal at the receiver side (input of the VTRx)
- the channel response equalization is required to provide sufficient EyeDiagram opening and therefore reliable data and clock recovery (CDR) at the data rate of 10Gbps
- the simulations demonstrate that a dedicated channel-response-equalizing CTLE circuit will significantly improve the performance of the data transmission link
- it is feasible to transmit the signals via a 40cm copper wireline Flex cable with the sufficient quality even at the data rate of 10Gbps (EyeDiagram opening : width=65ps p-p, height= 450mV p-p)