M.J. Rossewij

Electrical / piezo-resistive effects in bent ALPIDE – Monolithic Active Pixel (MAP) sensors

M.J. Rossewij[1], E. M. Okkinga[1], H. M. Naqvi[1], R. G. E. Barthel[1], S. R. Alving[1]

[1] *Utrecht University*

On behalf of the ALICE Collaboration

Introduction

The ITS3 design [1] foresees the replacement of the three innermost layers of the current ALICE tracker (ITS2) with wafer-scale stitched MAP sensors (65 nm) bent to cylindrical shapes. Multiple (beam) tests [2] with the existing ITS2 MAP (=ALPIDE chip, 180 nm) in bent state showed that the ALPIDE retains functionality and performance.

However, compared to the bending induced strain (ε=Δl/l≈0.1%), there was a relative large change (≈+10% or -5% depending on bending direction) in analog Power supply current (I_a). Gauge factor K= (ΔR/R)/ε≈-(Δ I_a / I_{a0})/ε of -100 or +50 strongly deviate from e.g. metals which are direction independent and typically around +2, mainly determined by the geometrical changes.

Strain effects in MOSFETs

Literature [3] mentions 2 effects on the MOSFET electrical properties:

1) Threshold shift: As strain affects the atomic lattice distances, the energy levels change including bandgap and MOSFET threshold V_{th}.

2) Piezo resistive effect: Changed energy levels also affects the mobility μ as 1) the effective mass **m*** is changed and 2) following the Boltzmann statistics, the charge carriers get redistributed over the energy levels. The piezo resistive coefficient **π** relates the applied stress **σ** with the change in resistivity **ρ** by:

$$-\frac{\Delta\mu}{\mu} \approx \frac{\Delta\rho}{\rho} = \boldsymbol{\pi\sigma} = \boldsymbol{\pi c\varepsilon} \qquad \mathbf{c}\text{=Stiffness}$$

Both effects affect the FET in e.g. saturation:

$$I_D = \frac{\mu\, COX}{2} * \frac{W}{L}[V_{GS} - Vth]^2[1 + \lambda\, VDS]$$

ALPIDE pixel biasing

The FETs in each pixel are biased with voltages and currents coming from central DAC circuitry (fig. 1) containing following 3 (8-bit) DAC types:

1) 5 Current DACs
2) 5 Voltage DACS with linear buffer
3) 4 Voltage DACs with Source Follower (SF)

All voltage DACs share same resistor divider. The DACMONV/I pins allow direct monitoring of one the voltage/current DACs

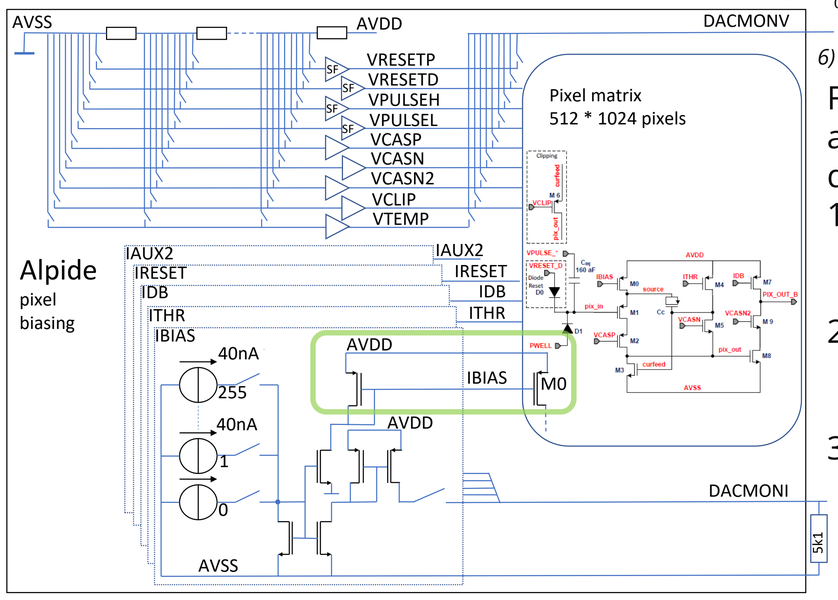
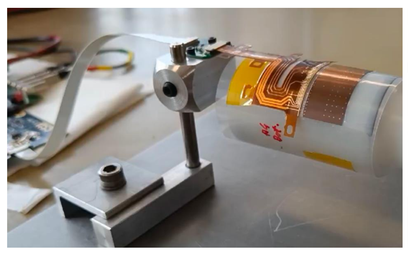


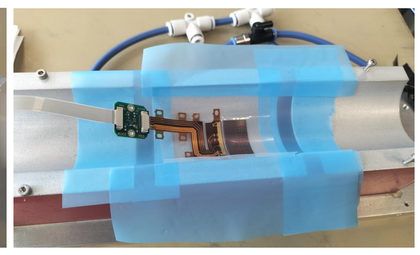
Figure 1): ALPIDE pixel biasing circuitry (all pixels share same biasing)

Measurement Setup

The measurement setup provides DACMONV/I access and allows convex (fig. 2) and concave (fig. 3) bending over long and short axis. The Alpide is glued on a plastic sheet which is bent over a mandril with curvature radii of 18, 24 and 30 mm as foreseen in ITS3. Concave bending employs porous aluminum profiles where vacuum keeps the Alpide-flex in place.



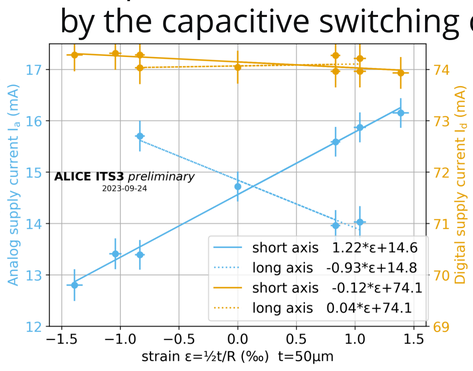
2) Short axis convex (ε>0, tensile) bending



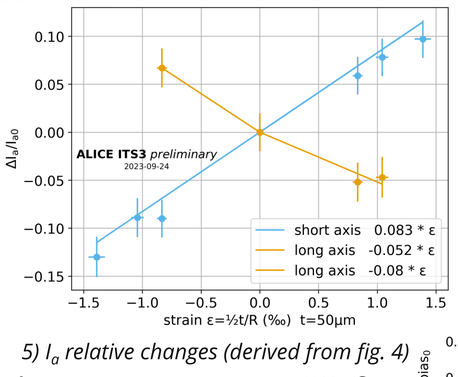
3) Short axis concave (ε<0, compressive) bending

I_a and I_d under bending

Figure 4 shows measured I_a and I_d for different strain values derived from the bent-radii using ε=½t/R [6], with t=thickness of the ALPIDE. Bending has strong effect on I_a while I_d is mostly unaffected, especially compared to its absolute value which is dominated by the capacitive switching current.



4) Measured I_a and I_d for different bent-radii

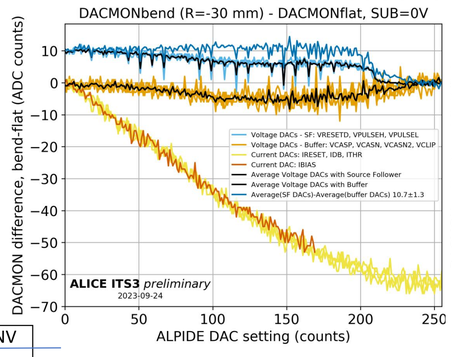


5) I_a relative changes (derived from fig. 4)

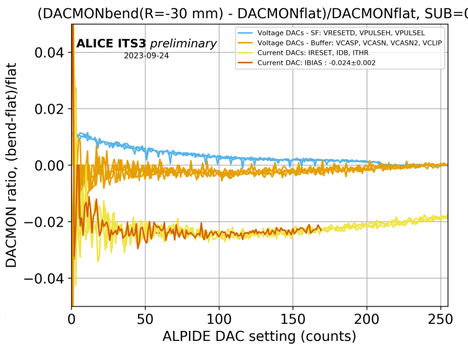
Figure 5 shows relative I_a changes, giving K=-83 for short axis. Long axis is asymmetric with K=+52 (ε>0).

DACMONV/I

To investigate to which level the I_a changes come from changes in the central DAC output, DACMONV/I was measured for all radii.



6) DACmonV/I difference for short axis R=-30



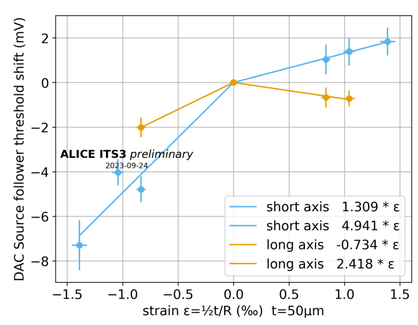
7) DACmonV/I ratio for short axis R=-30

Figure 6 shows the difference of DACMONV/I in flat and bent (R=-30, short axis) state. It clearly shows different responses from the 3 DAC types.

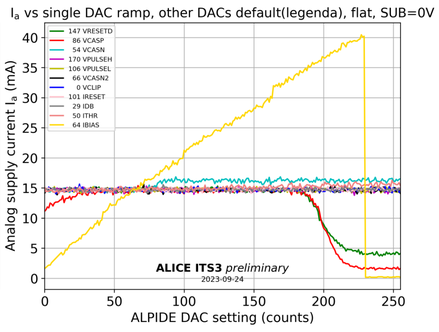
1) The current DAC difference decreases linearly up to DAC-value 150. This translates in a -2% change in the current DACs as shown in the figure 7.
2) The buffer voltage DACs all show the same slight deviations which are probably introduced by the shared resistor divider.
3) The SF voltage difference goes to 0 for DAC value >200 as it is below PMOS threshold. For DAC value <200, it seems rather straight, especially after correction with the averaged buffer voltage DACs values. This suggests it is also affected by the same errors from the shared resistor divider.

SF threshold shift

For all radii, the SF straight section is averaged from DAC value 0 to 170, scaled to an offset shift in mV and plotted in figure 8. The offset shift magnitude is in the same order as typical PMOS threshold shifts found in literature [4], however there are significant differences requiring a more in depth study [3, 5] to explain.



8) SF threshold shifts for different strain

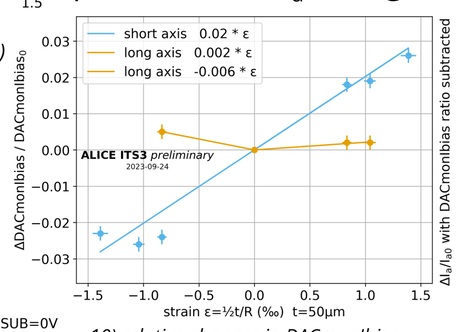


9) I_a measured for varying DAC settings

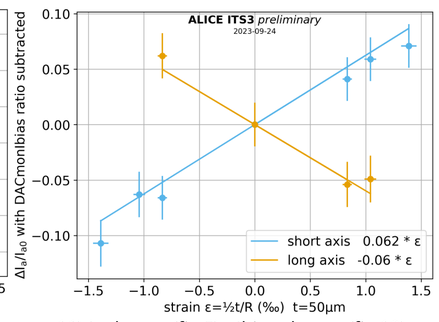
I_a changes disentangled from IBIAS-DAC

Figure 9 shows how I_a changes when ramping up one DAC while keeping others default. It shows I_a mainly/only depends on IBIAS in a linear way.

Figure 10 shows how DACmonIbias changes for different bending radii. As mentioned before this is ±1...2%, much lower than the ±5...10% I_a change. Subtracting DACmonIbias change from $\Delta I_a/I_{a0}$ gives figure 11 basically showing the effect of the circuitry after DACmonIbias (=buffering + pixels) on the I_a changes.



10) relative changes in DACmonIbias



11) I_a change (fig 5) - Ibias change (fig 10)

The long axis asymmetric behavior disappears and short axis gauge factors becomes smaller and similar to the long axis with opposite sign. Behavior like this is expected when current mirror FETs are rotated with each other [5]. Validating the design layout indeed revealed that FET M0 is rotated with respect to its counterpart (see green box fig. 1).

Conclusion

Though the ALPIDE in bent state remains fully functional, some electrical properties change most notably I_a. Above analyses showed that through the piezo resistive effect, rotation of current mirror FETs could be responsible which was confirmed after validating the design layout. It stresses the importance of maintaining the orientation in symmetric structures. There are also indication for bending induced threshold shifts in the source follower PMOS. To get more insight for ITS3, further research on the 65nm transistor test structures are foreseen.

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