BigRock, a Fast Timing Front End for Future Pixels in a 28 nm CMOS Process

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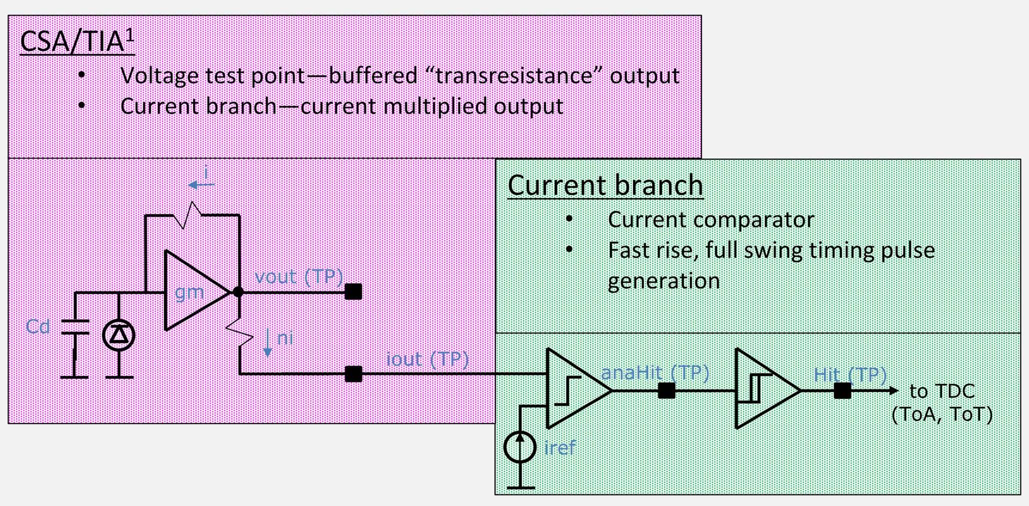
Summary

- Future tracking detectors for HEP will require both high time resolution and low power operation for 4D tracking at higher luminosity
- The higher bandwidth and increased density offered by smaller CMOS nodes is more suitable to enable enhanced pixel performance
- Smaller feature processes have lower process voltage, making current-mode design implementations attractive due to lower voltage swing
- Current-mode schemes also allow lower complexity of design implementations due to intrinsic gain scaling by transistor width selection
- In-silicon test results are not yet available**, simulation results** are covered herein

BigRock Analog Front End (AFE)

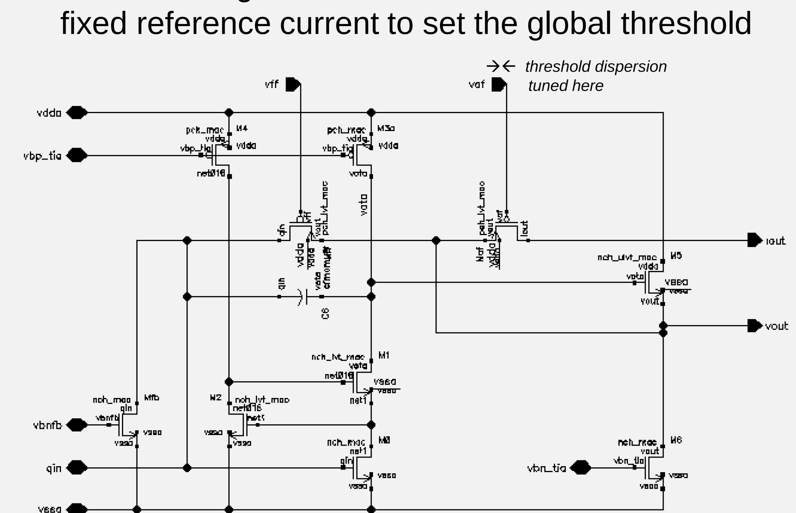
- The CSA topology follows the design described in ref. 1
- The BW of this design is not sufficient track the detector current pulse like a true TIA, as in 1
- However, the result is a very fast pulse peaking time (3-10 ns) that is optimal for low jitter
- The signal current presented to the current comparator is multiplied by ratio "n", where "n" is implemented as a transistor ratio and control voltage differential (next frame)



1. Pierre Jarron, et. al, *A transimpedance amplifier using a novel current mode feedback loop, 1996*

BigRock CSA

- The CSA is a typical regulated cascode design
- The input current pulse (charge) is mirrored forward to the current comparator as the signal
- The mirror factor is determined by ratio of *vaf, vff* and their respective transistor sizing *W, L*
- The next stage is a cascode current source with fixed reference current to set the global threshold



Pin	Function	Note
vbp_tia	CSA bias	Speed/power
vbn_tia	CSA follower bias	*
vaf	CSA current gain	+ Threshold tuning
vff	CSA feedback	Pulse gain/BW
vbnfb	Leakage current	+ Mfb op point
hit	ToA, ToT	*
iref	Global threshold	Set in i-comparator
vout(buf)	Test point	*
iout(buf)	Test point	*

Metric	Requirement	Simulated
Idc	~ 4 uA	6 uA
ToA S.D. (0.5 fC inj @ 0.15 fC)	~ 50 ps	50-60 ps
ENC	< 100 e RMS	80-90 e RMS
Threshold S.D.	*	…
Timewalk (1.2 ke – 30 ke)	*	~ 3.5 ns
ToT	*	2-20 ns
Area	< 30 x 30 um	10 x 30 um

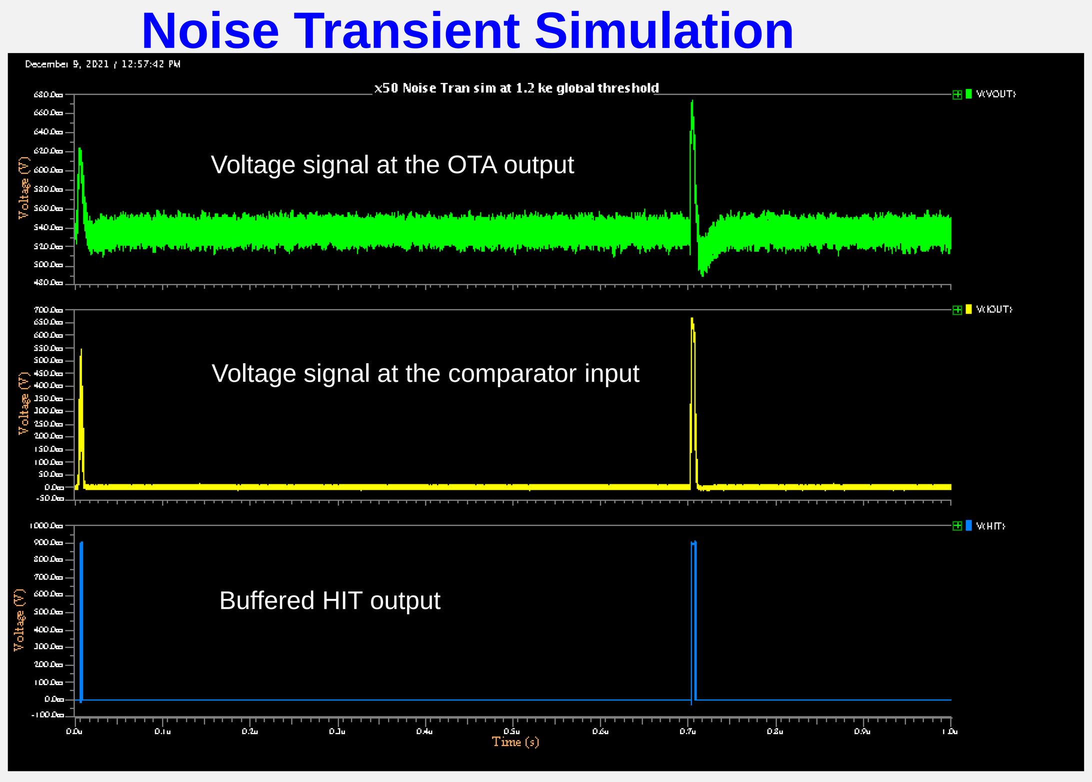
Essential requirements for a future pixel AFE

- µ-power preamp, ~ 50 ps timing resolution Time of Arrival (ToA)
- Charge readout for time walk correction → equivalent resolution ToT
- Target same sensor specification as HL-LHC
- Target same power and dimension as HL-LHC at higher logic density
- Digital: µ-power TDC, < 50 ps resolution (in-pixel TDC for next tapeout)

Essential requirements for AFE characterization

- On-chip testbench—TDCs (< 10 ps RMS) record ToA and ToT (~20 ns)
- Injection ckt—on the order hundreds e to 10 ke+
- Several channels, with some allowing buffered test points—TP above
- 1 GHz fast clock input for synchronous TDC & injection—LVDS receiver
- High speed test points buffered out—CML driver, analog buffer pads
- Core-voltage-only implementation for TID tolerance to 1 Grad+

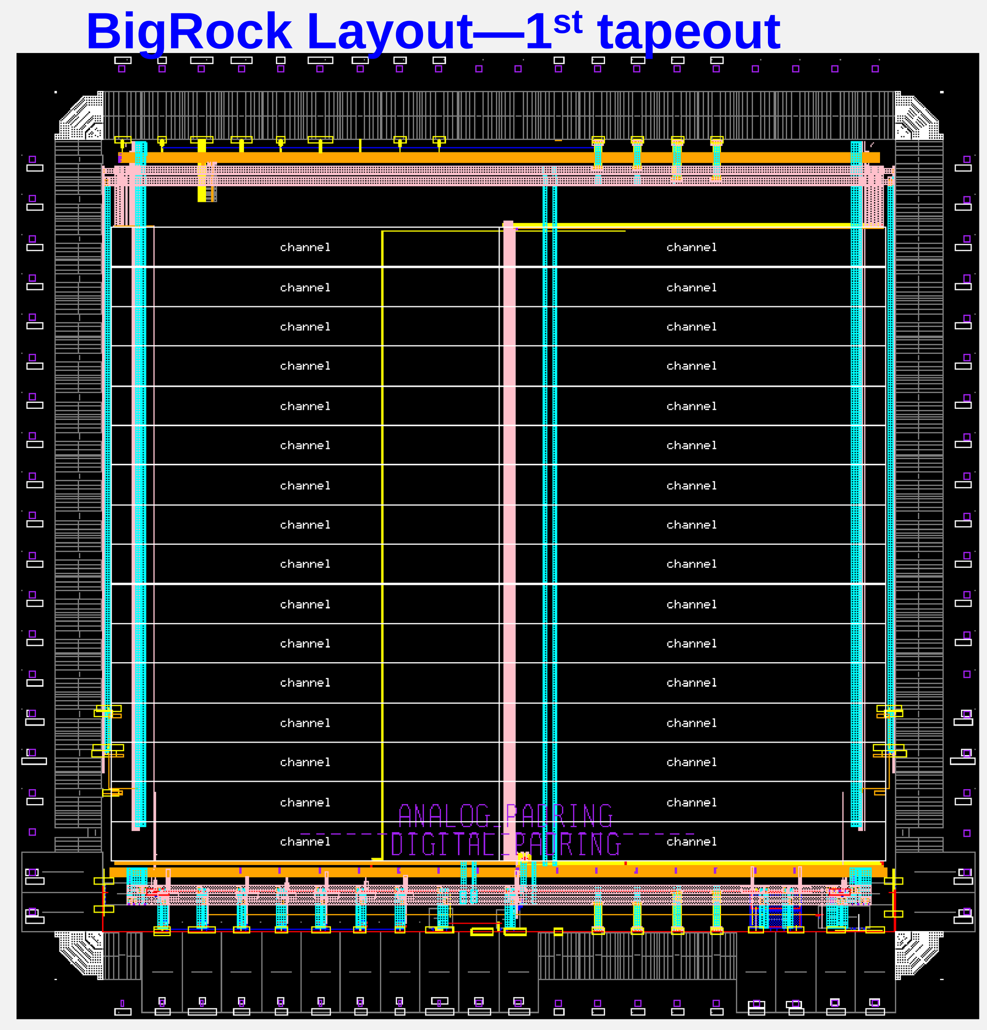
Noise Transient Simulation



Example Signal Chain

- A 1.2 ke at-threshold tuning pulse is followed by a 3 ke charge injection to represent a central charge deposition

BigRock Layout—1st tapeout



BigRock prototype

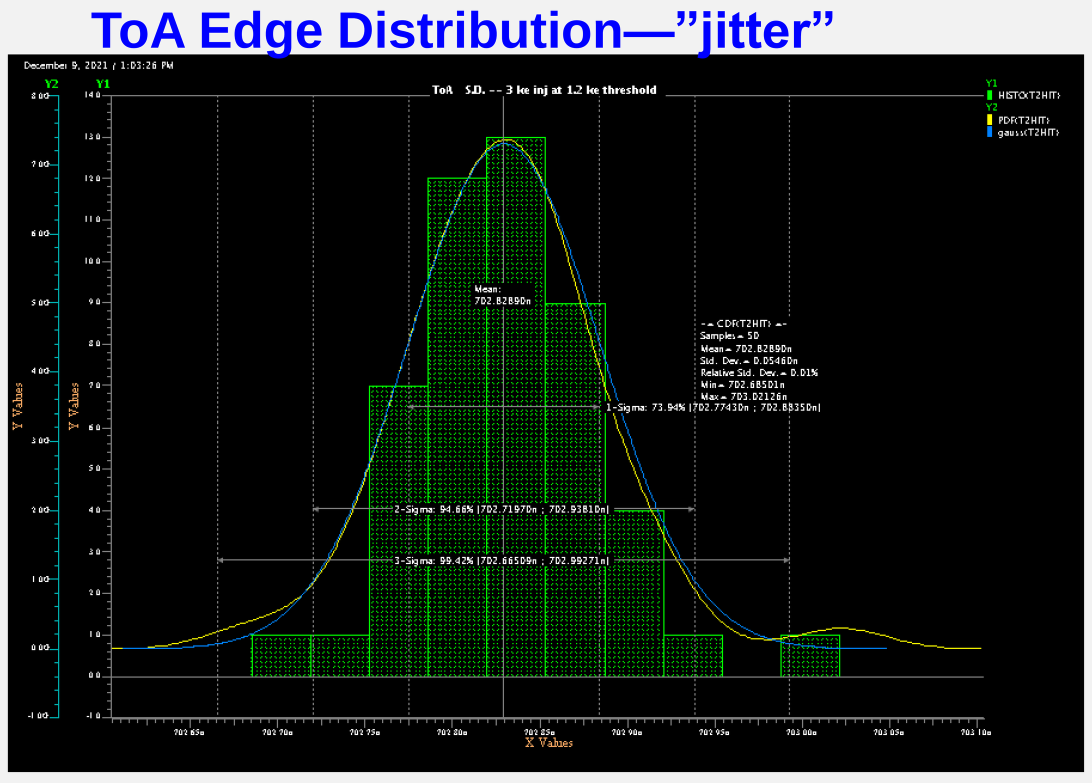
- 32 "channels" on 90 um pitch (pre-shrink)
- 16 channels per side
- 1 AFE per channel with calibration charge injection ckt
- 2 TDCs per channel—1 Start, 1 Stop
- All pads on 90 um pitch
- CLK receiver—LVDS
- CLKOUT monitor—CML driver
- 2 analog channels with buffered test points
- Preamp TP output—source follower, 2 pF drive capability
- Analog Hit output—source follower, 2 pF drive capability
- ToT pulse—CML
- 1 channels is connected to an input pad (300 fF)
- 0/25fF/50fF/100fF loading array for characterization (2nd tapeout)

BigRock Injection Ckt: 4 bits MoM cap + variable Vinj on base cell

BigRock TDCs

- INJ and TDC START are triggered by first 1 GHz CLOCK after PRIME
- TDCs count the number of 1 GHz clocks (up to 63), and …
- 1 GHz clock re-triggers a 128-stage delay line each period
- HIT rising edge from AFE stops the RISING EDGE TDC
- HIT falling edge from AFE stops FALLING EDGE TDC
- Each TDC output is
  - Number of clocks (6 bits), plus …
  - 128 delay line taps (find 1-0 transition for fine time resolution)

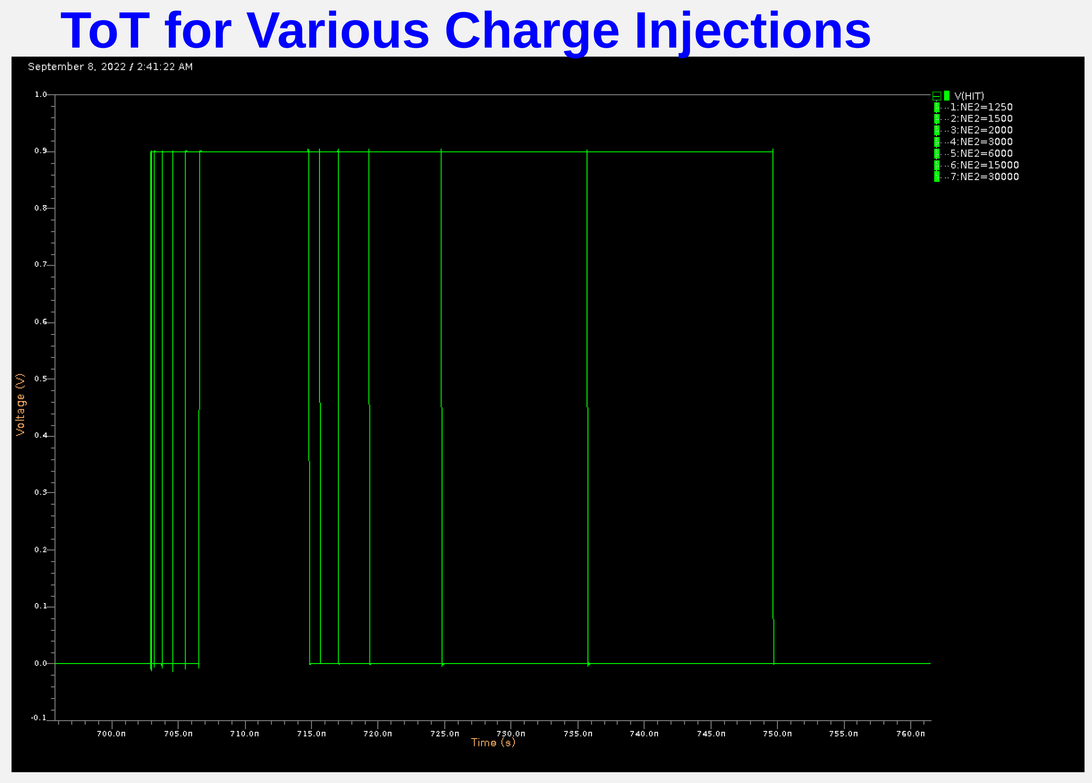
ToA Edge Distribution—"jitter"



Example of noise transient result for ToA

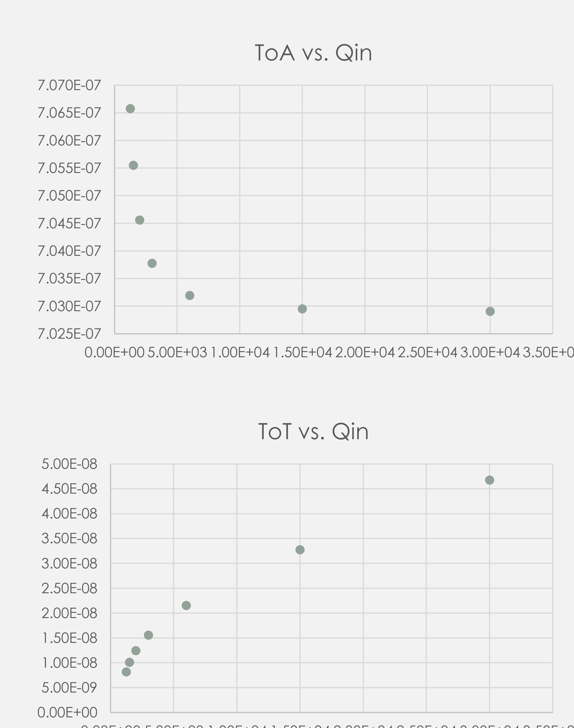
- The 3 ke leading edge transition is extracted from noise transient simulations
- The S.D of the rising-edge timing distribution gives the jitter (54 ps RMS)

ToT for Various Charge Injections

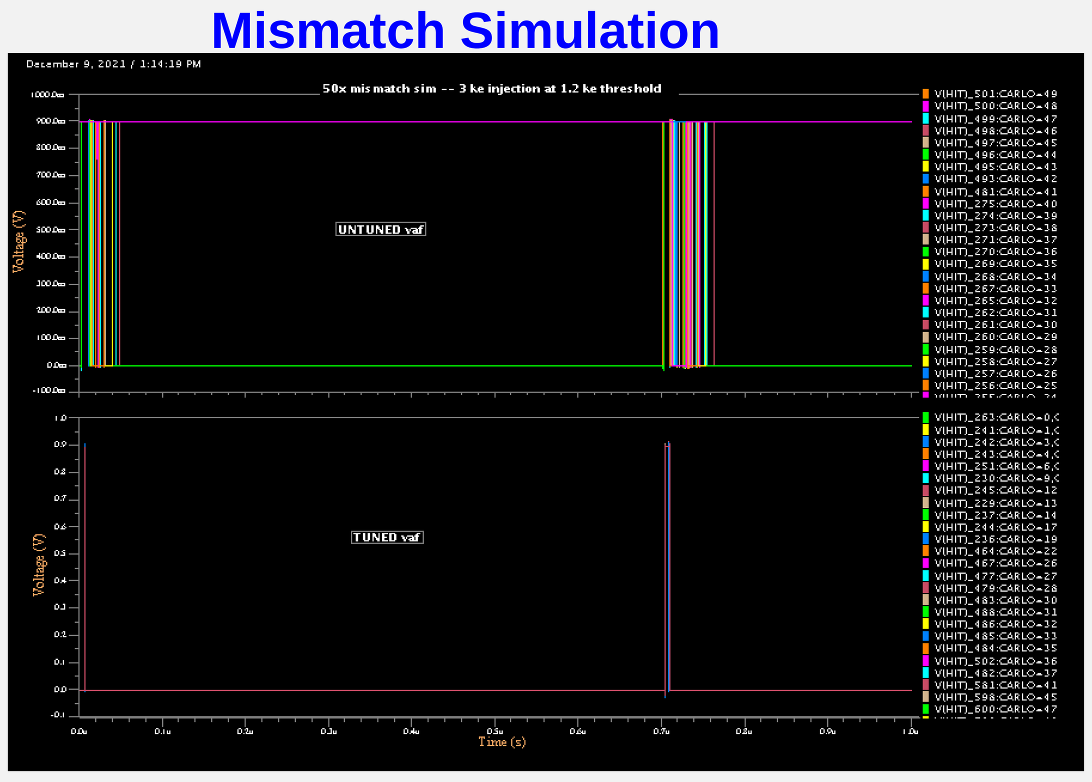


Example of ToT vs. input charge

- Allows extraction of timewalk and ToT linearity



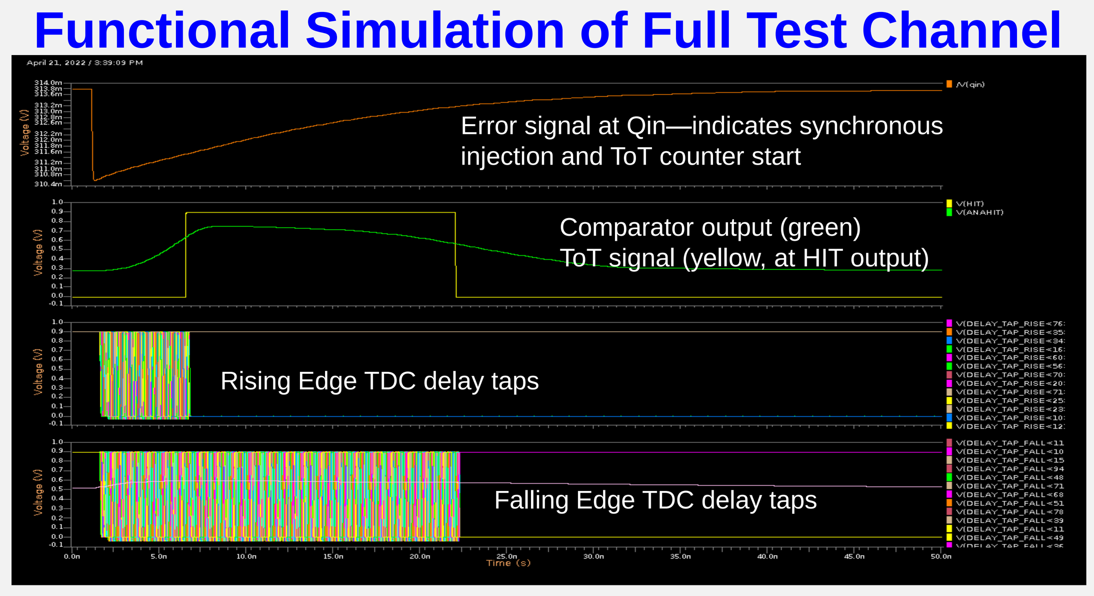
Mismatch Simulation



Example of tuning pixel threshold offsets

- Threshold tuning algorithm implemented in an Eldo script
- Tuning is performed as minimum detectable pulse present at 1.2 ke injection
- Result indicates that a trim of 100 mV will be required, with a precision of 2 mV

Functional Simulation of Full Test Channel



Injection sequence for a channel

- A channel is one AFE pixel, plus two TDCs
- An enable signal, PRIME, allows a synchronous trigger of both the injection circuit and the rising and falling edge TDCs
- The edges are recorded by the TDCs with ~ 5 ps resolution, for a period of up to 63 ns
- The two frozen counter values are read out serially