Characterization of the BigRock 28 nm Fast Timing **Analog Front End**

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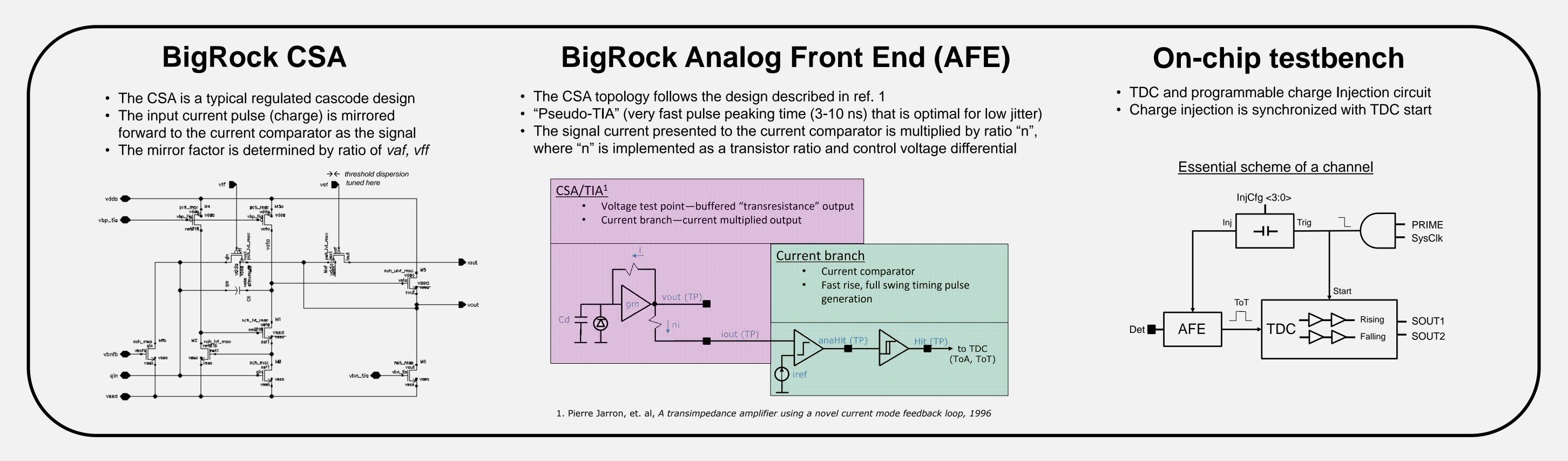


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Summary

A succession of design refinements have been implemented in a common 2x2 mm 28 nm testbed ASIC series—BigRock, Pebbles, and MetaRock. Pebbles, the device now being characterized in the lab, implements an array of on-chip input capacitor loads for characterizing the BigRock AFE performance from 0 to 100 fF. Noise, ToA and ToT timing dispersion, ToT-vs-Qin, and timewalk are covered herein. MetaRock (FY24) is the final prototype in the series. It features a more efficient, faster revision of the BigRock CSA, and includes a full timing and charge readout AFE with a new low power analog TDC suitable for implementation in a next-generation pixel readout ASIC for HL-LHC upgrades or other 4D tracking applications.



Goals of the 28 nm AFE prototype project

- Analog current consumption of ~ 4 uA
- Noise < 100 e- RMS @ 50 fF detector capacitance
- ToA requirement of ~ 50 ps RMS resolution for 4D tracking
- ToT precision commensurate with timewalk correction
- Performance met at 0.15 fC threshold with 0.5 fC charge injection
- On-chip testbench— high-resolution TDCs record ToA and ToT
- Synchronized on-chip injection ckt—on the order 100's e to 20 ke+
- Several channels, with some allowing buffered test points—TP above

Calibration of the fabricated on-chip testbench TDC

- High speed test points buffered out—CML driver, analog buffer pads
- Core-voltage-only implementation for TID tolerance to 1 Grad+

Pebbles on test PCB

chip Testbench TDC: 10 um x 500 um

Functional simulation of a channel

- Synchronous trigger of the injection circuit and ToA, ToT TDCs
- ToA and ToT edges are captured by 6-bit counter and 128-bit delay line Counter value and therrmomter code delay line bits are read out serially

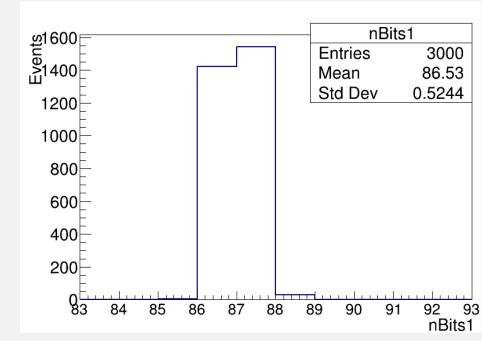
Vout at preamp Comparator output 500.0m 200.0m -100.0m Injection trigger—"PRIME" ToT pulse Rising edgeTDC delay taps Falling edgeTDC delay taps

Calculation of the timestamp

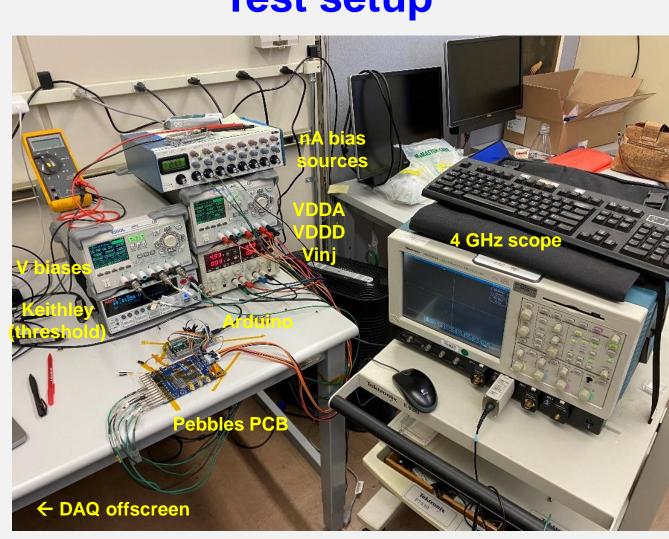
- Calibrate the delay line to get the delay time of one cell dT Giving tap[127:0] and count[5:0]:
- Count number of consecutive 1s and 0s in tap[127:0], for 001111111111111111111111111111111 11111111111111111111111111111100
- Gives us nBits = [66, 60, 2], note that for the clock frequency we chose (clock period Tc < 128*dT), it is guaranteed that we will see at least 3 blocks of 1s and 0s
- If tap[0] == 1: TOA = count[5:0]*Tc + dT*nBits[-1] • If tap[0] == 0: TOA = count[5:0]*Tc + dT*(nBits[-1] + nBits[-2])
- TOT is just the difference of the two TOAs
- SOUT2 and SOUT1

Measuring delay cell dT

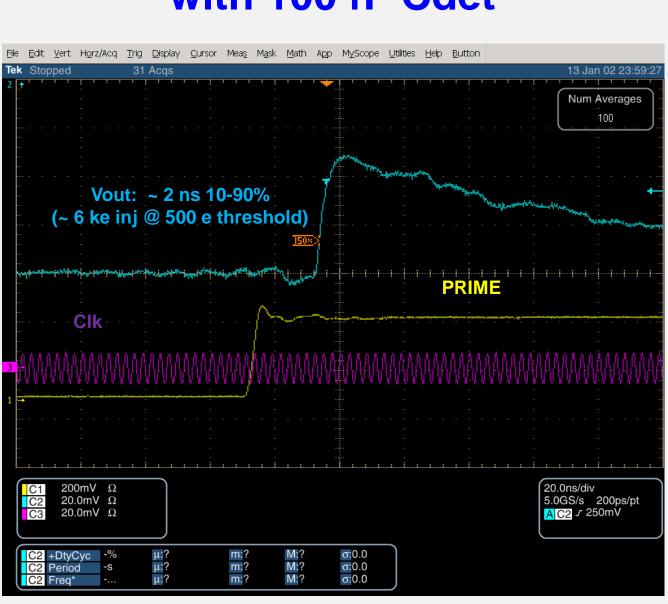
- With 528 MHz clock (Tc = 1.89 ns), measure the number of delay bits in a complete clock cycle
- Measured delay per bit: 21.89 ps



Test setup



Preamp Vout TP with 100 fF Cdet



Measured performance parameters at ~ 1 ke threshold (+/- 25% charge injection uncertainty)

