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Characterization of the BigRock 28 nm Fast Timing Analog Front End

Tuesday, 3 October 2023 15:00 (20 minutes)

A full characterization of the BigRock high-speed, low-power analog front end (AFE) will be presented. The BigRock AFE previously described in [1] has been refined in a second generation testbed ASIC, Pebbles. The AFE utilizes a current-mode signal path that has been designed for 4D tracking applications with precision time resolution of order 50 ps. The preamplifier concept is based on a prior art current-feedback CMOS topology in [2]. An on-chip test bench comprised of a variable injection circuit and high-resolution TDC measures the AFE timing resolution. An array of integrated load capacitors and IO IPs enhance the characterization capability.

Summary (500 words)

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A succession of design refinements have been implemented in a common 2x2 mm testbed ASIC series. The family of 28 nm CMOS prototype ASICs, from initial to final are: BigRock, Pebbles, and MetaRock. The 1st chip in the series, BigRock, contains an IO design flaw that renders it untestable, as well as a bug in the digital TDC. Pebbles, the device now being characterized in the lab, ameliorates these flaws, and implements an array of on-chip input capacitor loads for characterizing the BigRock AFE noise from 0 to 100 fF. In this presentation, the critical metrics of noise-vs-power, timing dispersion, threshold tuning, ToT-vs-Qin, and timewalk will be covered.

The final prototype in the series, MetaRock, will be taped-out in June of 2023. MetaRock will have a full timing and charge readout AFE based on BigRock, including a new low power analog TDC suitable for implementation in a next-generation pixel readout ASIC for HL-LHC upgrades or other 4D tracking applications.

Background

The intent of the BigRock project is to develop a next-generation AFE capable of approximately the same performance requirements as the recently designed ItkPix/CROC readout for the HL-LHC upgrade, but adding a timing requirement, and at the new CERN/HEP target node of 28 nm for increased digital capability. The BigRock module of the Pebbles ASIC is comprised of 17 channels with two main modules:

• An AFE consisting of a preamplifier, comparator, and digital buffer

• An injection circuit and dual TDC with ˜ 5 ps resolution, recording the ToT leading and trailing edge time referenced to a 1 GHz synchronous system clock

A low-power TDC will be a follow-on development included in the MetaRock tapeout, to complete the 4D front end. In the Pebbles iteration reported here, the channel TDC is intended only as an on-chip testbench for the AFE, avoiding timing uncertainties in the interface and test PCB. Therefore, the TDC in this prototype is essentially unconstrained in design parameters, excepting resolution. The digital TDC is described in [3].

A preamplifier based on the prior art in [2] is the central element of the BigRock prototype project. The analog requirements are namely:

• analog current consumption of ˜4 uA

• noise < 100 e- RMS @ 50 fF detector capacitance

• ToA requirement of ˜50 ps RMS resolution for 4D tracking

• ToT precision commensurate with timewalk correction

• performance met at a 0.15 fC threshold with 0.5 fC central charge injection

[1] Amanda Krieger, Kennedy Caisley, Maurice Garcia-Sciveres, Carl Grace, Timon Heim, "BigRock, a Fast Timing Front End for Future Pixels in a 28 nm CMOS Process, Conference poster,"TWEPP 2022.
[2] Pierre Jarron, Francis Anghinolfi, Eric Delagne, Wladek Dabrowski, Luitwin Scharfettera, "A transimpedance amplifier using a novel current mode feedback loop", NIM-A, 377 (1996), pp. 435-439.
[2] Kennedy Caisley, "A Monolithic Radiation-Hard Testbed for Timing Characterization of Charge-Sensitive Particle Detector Front-Ends in 28 nm CMOS", Master of Science Thesis, Graduate Program in Electrical and Computer Engineering, The Ohio State University, 2021.

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