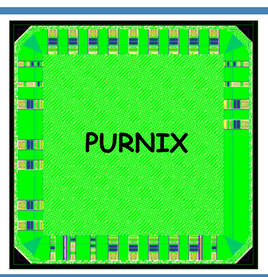
Science and Technology Facilities Council

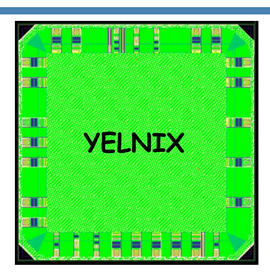
stfc.ukri.org

A Radiation Hardened IP Development Programme for 28nm CMOS Technology

Thomas Gardiner – Thomas.Gardiner@stfc.ac.uk, Oliver Bowett – Oliver.Bowett@stfc.ac.uk, Stephen Bell – Stephen.Bell@stfc.ac.uk, Alicja Michalowska-Forsyth – Alicja.Michalowska@tugraz.at
Jake Knight, Alex Steven, Mark Prydderch, Giulio Villani, Dan Beckett
STFC, Rutherford Appleton Laboratory, Harwell Campus, Didcot, Oxfordshire OX11 0QX, United Kingdom



The ASIC Design Group at RAL has commenced a three-year programme developing radiation-hardened 28nm circuits intended to provide verified building blocks for future projects. The aim of this programme is to complement and add to the CERN common IP library for 28nm. Our programme includes a range of utility circuits such as high precision amplifiers, a low power 12bit ADC for housekeeping, bandgaps, reference drivers, DACs, a 1Gbps Serializer for low-complexity readout, and more. To explore the benefits of the 28nm technology, a high-resolution LGAD front-end including a 20ps resolution TDC is also under development.



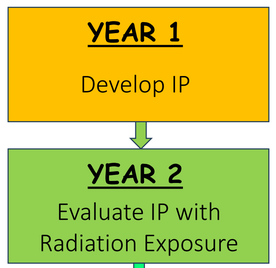
Introduction

This poster presents the progress made after one year in the three year programme to develop 28nm radiation hardened IP in 28nm CMOS technology with a maximum radiation dose of 1GRAD TID.

Objectives of the programme are to gain an in-depth understanding and knowledge of 28nm CMOS technology when operating in harsh radioactive environments and the production of a range of verified radiation hardened IP to act as building blocks for new ASICs. Furthermore, a LGAD front-end 28nm ASIC is in development as real applicable use of this IP.

All developed IP use layers M1-M5 and to minimise radiation damage performance effects; minimum transistor width of 1µm and maximum length of 500nm are implemented. Digital circuits use 12T libraries with all control circuitry being fully triplicated.

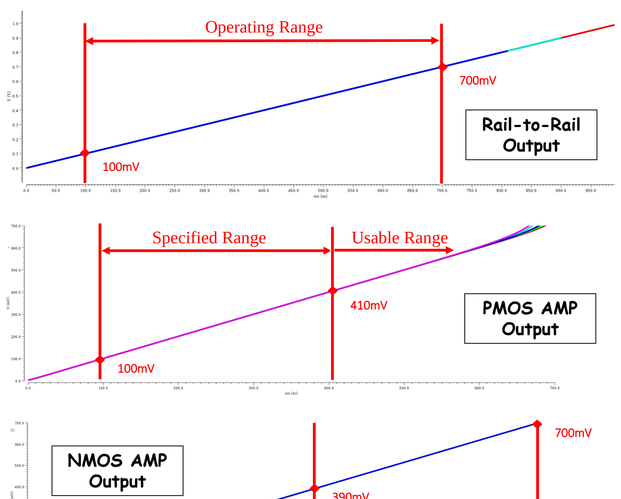
2 test structure ASICs are set for fabrication in 25th October 2023:
PURNIX ASIC – ASIC containing a range of generic prototype IP
YELNIX ASIC – ASIC containing prototype IP for the LGAD frontend ASIC



Amplifier IP

A range of amplifiers have been developed to validate the analogue technology limits of 28nm CMOS.

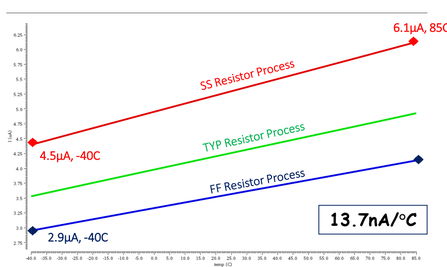
- Rail-to-Rail class AB Precision Amplifier
  - <800µW power consumption
  - 70x42um²
  - Input range of 100-700mV
  - Input offset <3mV
  - High drive strength for high loads on-chip/off-chip
- PMOS input class AB High speed Amplifier
  - <700µW power consumption
  - 63x53um²
  - Input range of 100-410mV
  - Bandwidth 100MHz at 1pF load
  - Input offset <5mV
  - High speed for driving fast signals or references.
- NMOS input class AB High speed Amplifier
  - <700µW power consumption
  - 60x40um²
  - Input range of 390-700mV
  - Bandwidth 100MHz at 1pF load
  - Input offset <5mV
  - High speed for driving fast signals or references.



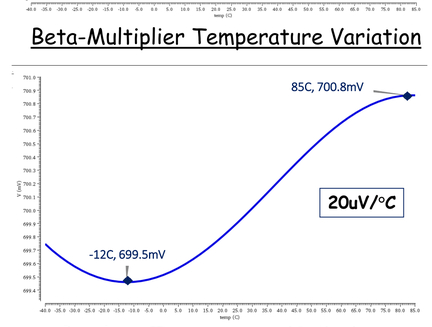
Beta Multiplier + Voltage Bandgap IP

Fluctuations in self-generation current and voltage circuitry due to radiation damage can be critical problem and needs to be understood early on. A beta multiplier for self-current generation and a bandgap for self-voltage generation have been developed.

- Beta Multiplier
  - <170µW power consumption
  - 45x32µm²
  - Trimmable Output current 2.9-6.1µA
  - Supply + Transistor Process independent
  - <13.7nA/°C gradient
  - <5nA rms
- Voltage CMOS Bandgap
  - <90µW power consumption
  - 200x200um²
  - <20µV/°C gradient
  - Trimmable output voltages 100mV + 700mV
  - Output noise 70µVrms + 230µVrms respectively



Beta-Multiplier Temperature Variation

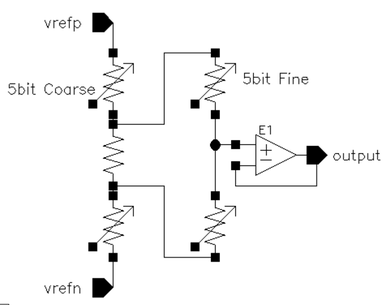


Bandgap Temperature Variation

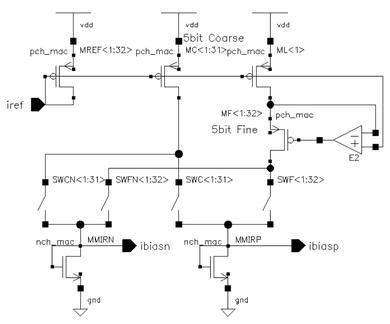
VDAC + IDAC IP

Voltage and Current DACs rely heavily on low-leakage switches for good performance, however with high radiation dosage, transistor leakage becomes a significant challenge. DAC IP has been developed to evaluate this issue specifically.

- 10bit resistor segmentation Voltage DAC
  - <800µW power consumption
  - 80x80um²
  - Output voltage 100-700mV
  - 1LSB DNL
  - 5LSB INL
- 10bit Mirroring Segmentation Current DAC
  - <100µW power consumption
  - 150x120um²
  - Differential Output Current 0-50uA
  - 4LSB DNL



VDAC Architecture



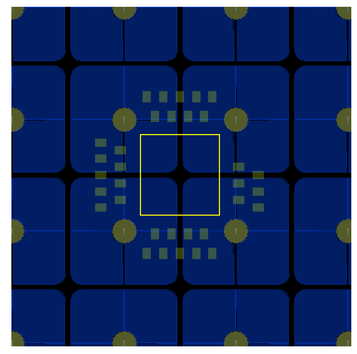
IDAC Architecture

LGAD Frontend

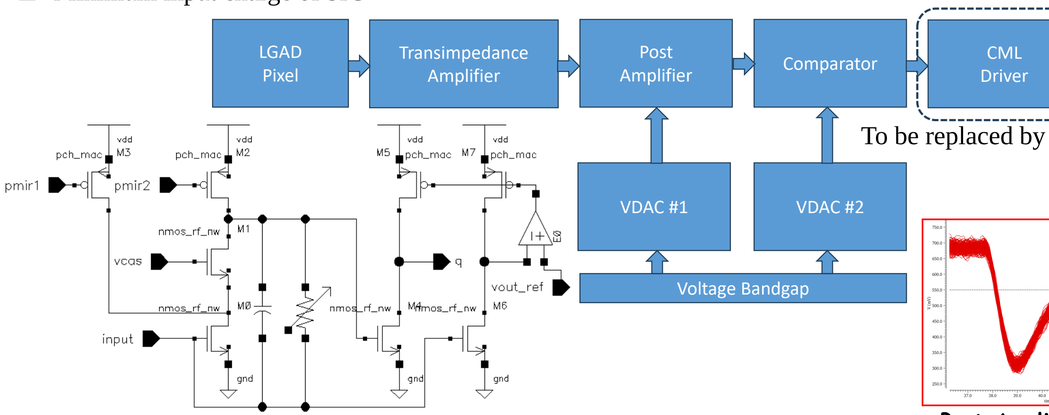
An LGAD frontend is in development for a 15x15 LGAD Array with pixel size at 1.3 × 1.3 mm².

An experimental application is to deploy 64 X 4ch 1mm² frontend test ASICs to service a 15x15 LGAD sensor. This is with an interposer PCB with the LGAD sensor bump-bonded on one side and the ASICs wire-bonded on the other with the sensor connection going through a staggered PCB VIA.

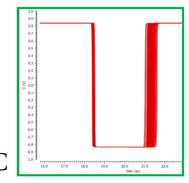
Requirements:
- ❑ <20ps rms Time of Arrival (TOA) resolution.
- ❑ A Time over Threshold (TOT) measurement.
- ❑ Minimum input charge of 3fC



LGAD PCB Design



LGAD Frontend Architecture



CML Output

Post Amplifier Output

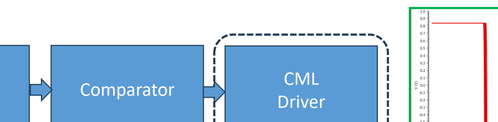
Sub-20ps TDC

Time-to-Digital-Converters (TDC) are extremely sensitive circuits. PDK models can predict most permutations however radiation damage performance loss and inaccurate parasitic extraction often lead to under-predicted performance.

Given the potential TDCs have for future development, 2 prototype sub-20ps TDC IPs are being trialled:
1) Coarse + Fine Vernier Delay Line Architecture
2) 12-stage Ring Oscillator PLL @ 2.56GHz

Prototype Vernier TDC Test Setup

Prototype PLL TDC Test Setup

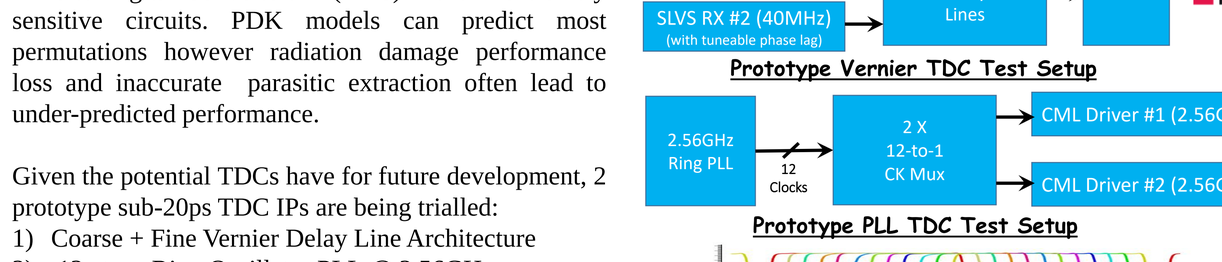


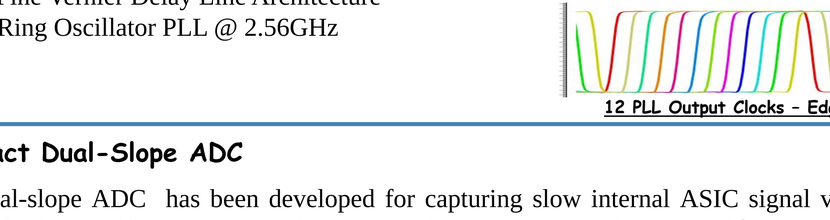
12 PLL Output Clocks – Edge separation 16.3ps

12bit Compact Dual-Slope ADC

A compact dual-slope ADC has been developed for capturing slow internal ASIC signal variations. This prototype ADC achieves 12bit resolution through multi-sampling averaging with self-calibration - this takes advantage of the high-speed low-area 28nm technology.

- ❑ 230x230um²
- ❑ Dual-slope Architecture
  - High R, low C time constant to keep area compact
  - 1GHz clock required to achieve 12bit with small time constant/area
  - Non-inverting integrator implemented to avoid mid-code boundary issues
- ❑ <5uA reference current consumption
- ❑ Self-digital calibration through high-precision resistive string
- ❑ 64 multi-sample capacity built in
  - <16 sample averaging required for 12bit (noise simulations)

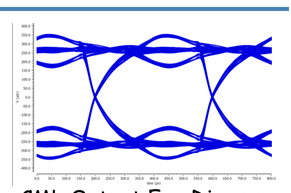




ADC Dual-Slope Architecture

SLVS RX + CML TX + DIGITAL

High speed digital circuitry is becoming more critical as technology nodes shrink, IP has been developed to validate high frequency performance in respect to radiation damage. High frequency clocks (<2GHz) are transferred in to perform digital tasks in fully triplicated digital logic and the output raw data is readout serially through high speed links. This IP includes AC-coupled SLVS receiver, PRBS+Multiplier triplicated circuitry and CML drivers.



CML Output Eye Diagram