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A Radiation Hardened IP Development Programme for 28nm CMOS Technology

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The ASIC Design Group at RAL has commenced a three-year programme developing radiation-hardened 28nm circuits intended to provide verified building blocks for future projects. The aim of this programme is to complement and add to the CERN common IP library for 28nm. Our programme includes a range of utility circuits such as high precision amplifiers, a low power 12bit ADC for housekeeping, bandgaps, reference drivers, DACs, a 1Gbps Serializer for low-complexity readout, and more. To explore the benefits of the 28nm technology, a high-resolution LGAD front-end including a 20ps resolution TDC is also under development.

Summary (500 words)

We will present the programme and the expected performance of completed 28nm circuits scheduled to be fabricated in October 2023.
28nm CMOS is a key technology for designing operational ASICs for future experiments in HL-LHC, this is due to the need of superior radiation tolerance in comparison to older technologies. The ASIC Design Group at Rutherford Appleton Laboratory has commenced a three-year programme developing radiation-hardened 28nm circuits intended to provide verified building blocks for future projects. Target radiation hardness for these circuits is 1Grad Total Ionization Dose (TID).
The aim of this programme is to complement and add to the CERN common IP library for 28nm CMOS. The CERN common IP library has specification standards for our IP to be accepted; this operational process-voltage-temperature variations, limited transistor flavours and maximum number of routing layers. All our designed IP has this requirement built into the specification.
Our programme includes a range of utility circuits such as high precision amplifiers, a low power 12bit ADC for housekeeping, bandgaps, reference drivers, DACs, a 1Gbps Serializer for low-complexity readout, and more. To explore the benefits of the 28nm technology, a high-resolution LGAD front-end including a 20ps resolution TDC is also under development.
This submission will present the goals and milestones of the programme and highlight the completed 28nm circuits which are designed to be radiation hardened and meet the CERN common IP library requirements.

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