

Beam test of a baseline vertex detector for the CEPC

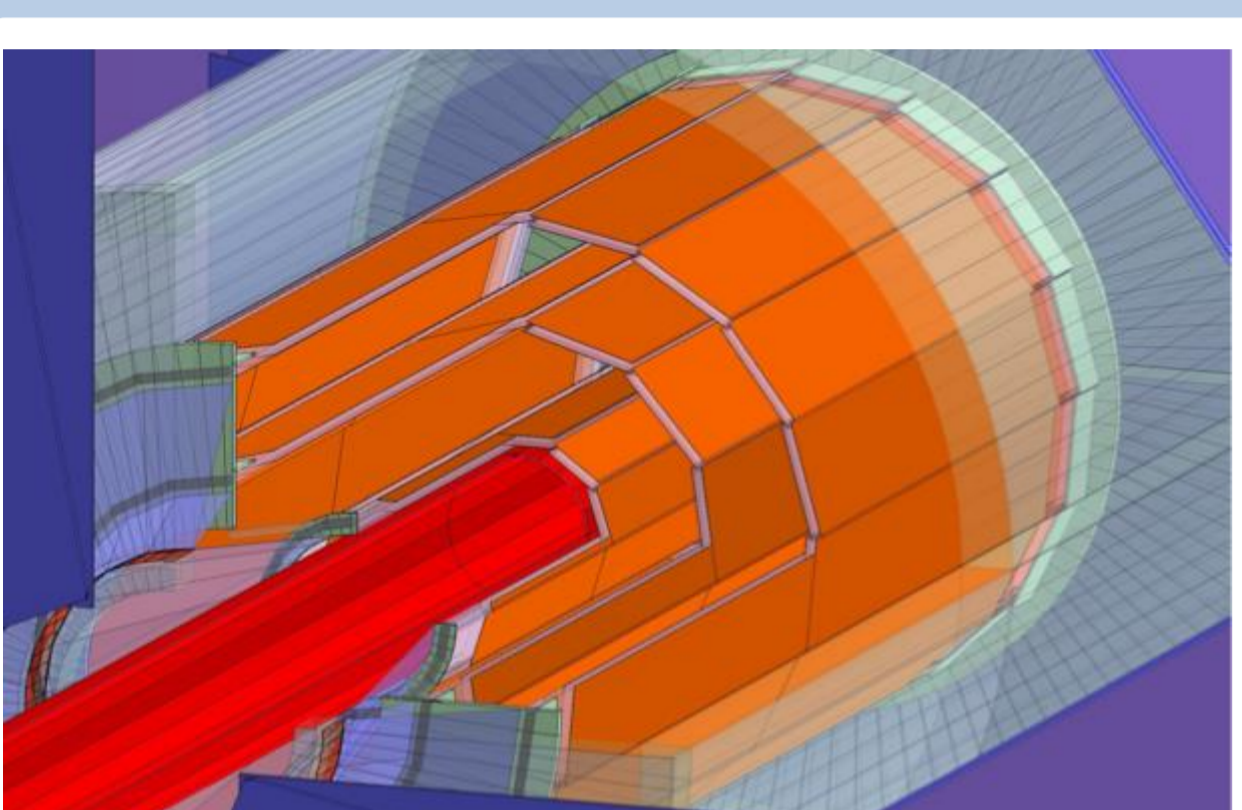
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Abstract

- The proposed Circular Electron Positron Collider (CEPC) presents challenges for the vertex detector in terms of material budget, spatial resolution, readout speed, and power consumption.
- A Monolithic Active Pixel Sensor (MAPS) prototype called TaichuPix has been implemented, which has been characterized by a spatial resolution of less than 5 μm and a detection efficiency better than 99 %.
- The baseline vertex detector is proposed with a three-ladder architecture, which is double-sided with TaichuPix sensors.
- Six ladders were installed on the barrel, and the beam test was conducted at the DESY II TB21 facility.



Schematic of a baseline vertex detector for the CEPC

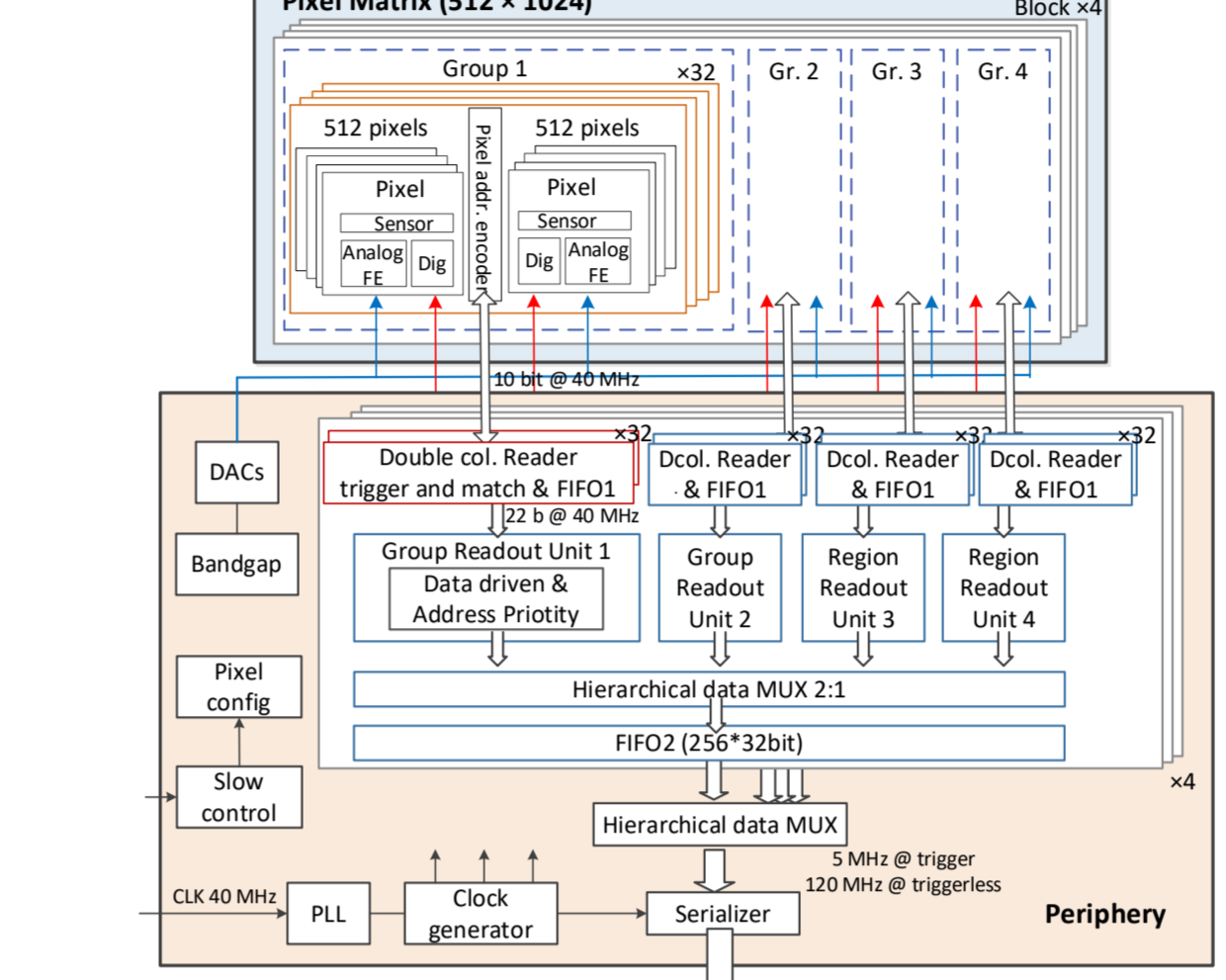
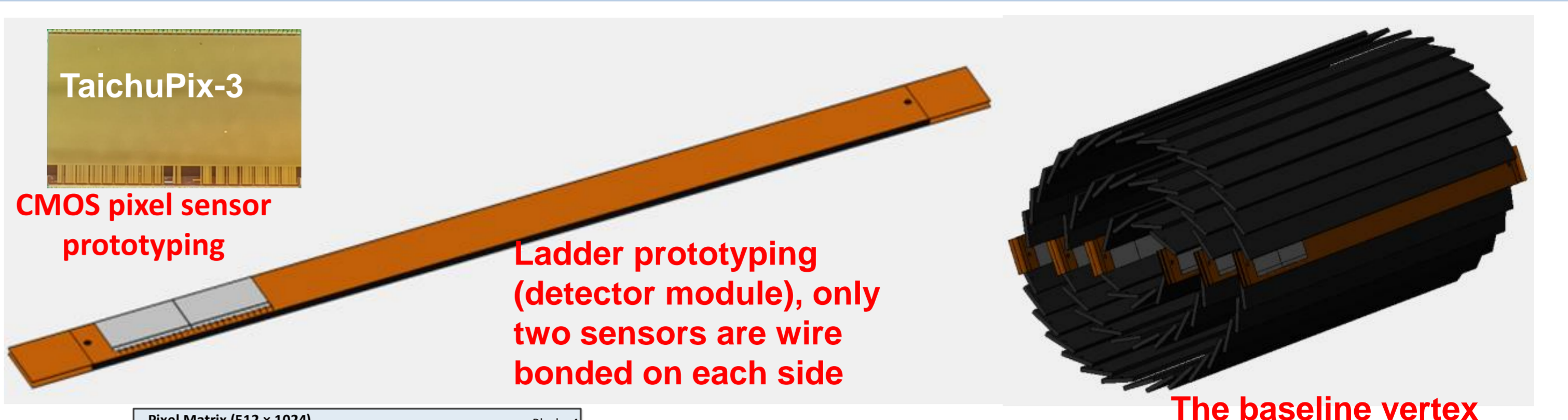
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Motivated from CEPC CDR:

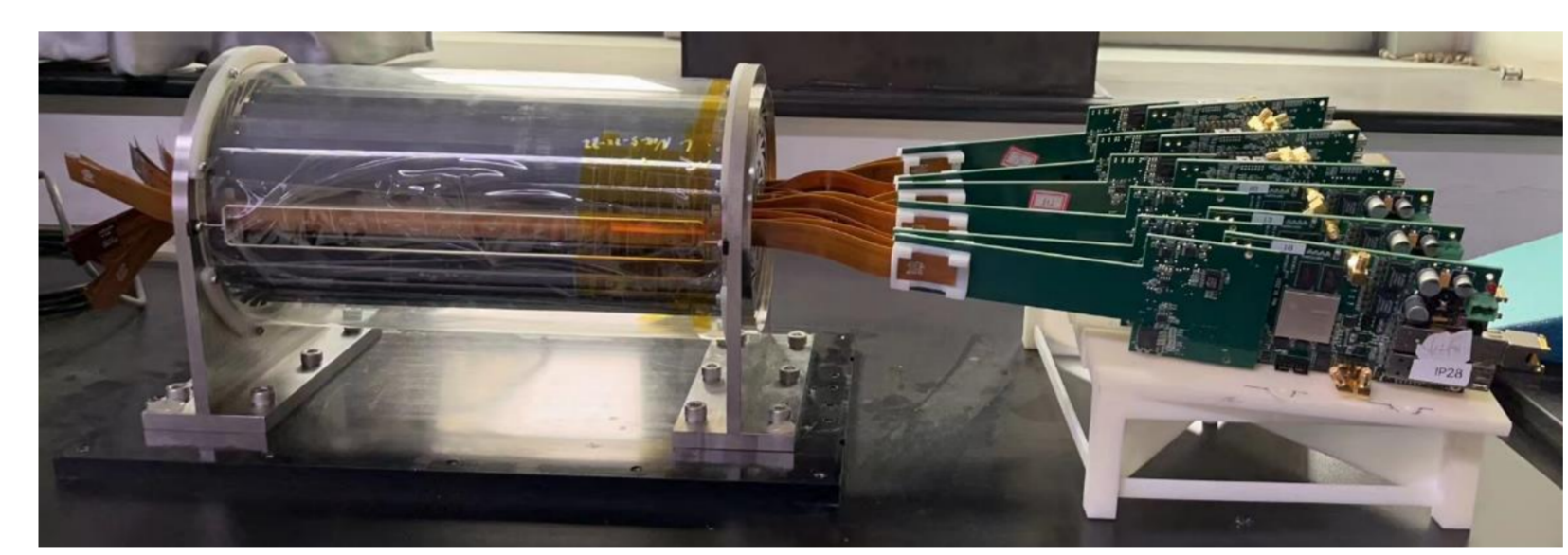
- Critical to provide excellent impact parameter resolution
- First layer located at a radius: ~ 1.6 cm.
- Single-point resolution: $< 3 \mu\text{m}$. $\sim 16 \mu\text{m}$ pixel pitch
- Material budget: $< 0.15\% X_0/\text{layer}$.
- Power consumption: $< 50 \text{ mW}/\text{cm}^2$, if air cooling used
- Radiation hardness: 1 Mrad/year

CEPC baseline vertex detector prototype:

- three-ladder architecture
- Double-sided pixel sensors to each ladder
- Six precise reconstruction points

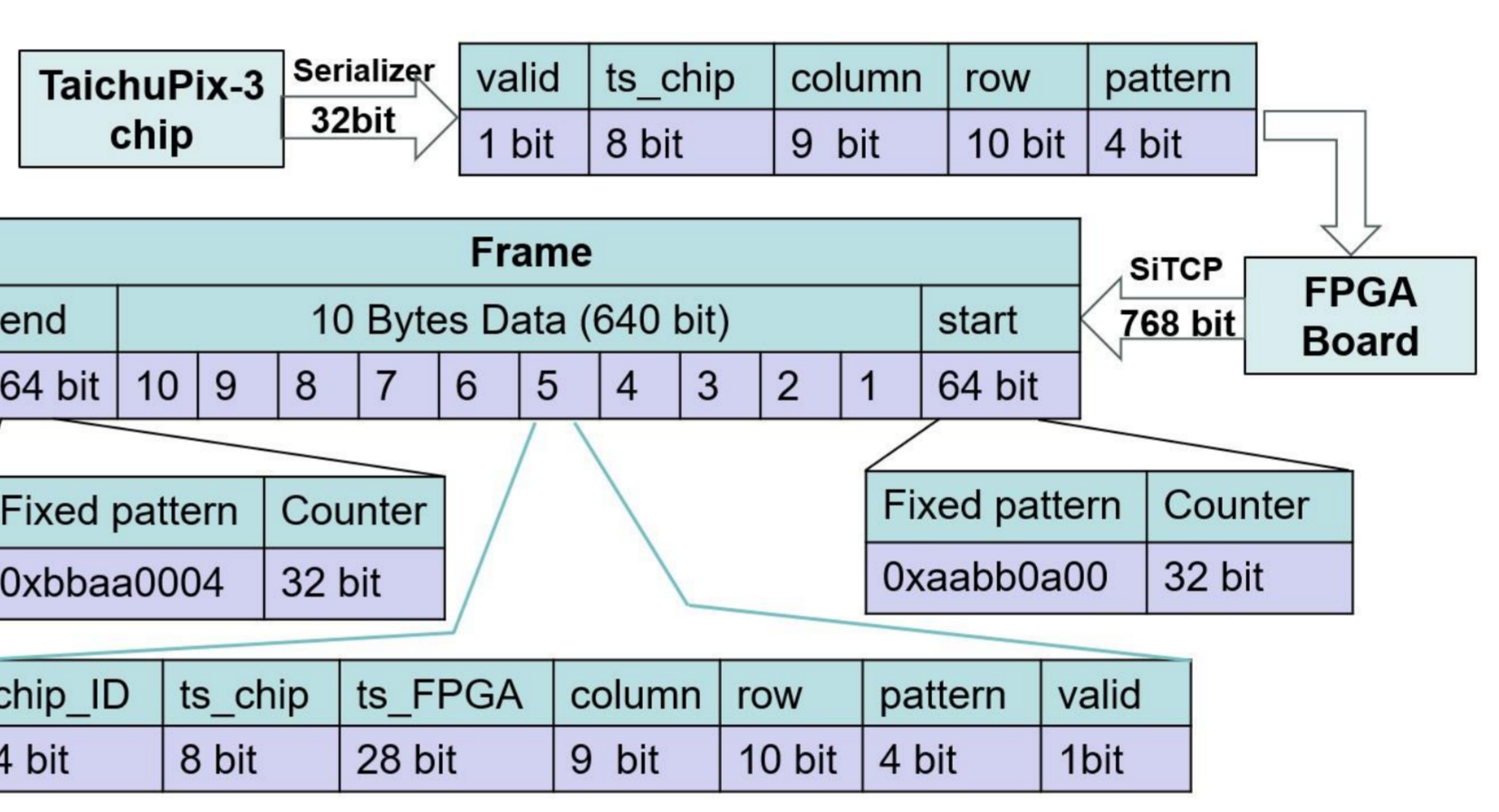


- TaichuPix-3**
- Chip size: $\sim 1.4 \times 2.56 \text{ cm}^2$
 - Pixel size: $25 \mu\text{m} \times 25 \mu\text{m}$
 - Pixel matrix: 512×1024
 - Technology: 180nm CIS process, including partial depletion and full depletion process.
 - Readout: Column-drain readout for pixel matrix, two-level FIFO architecture
 - Trigger-less and Trigger mode are compatible (max. 160Mbps for trigger mode & max. 3Gbps for triggerless)
 - Power density: Max. $200 \text{ mW}/\text{cm}^2$



Baseline vertex detector prototype with readout boards

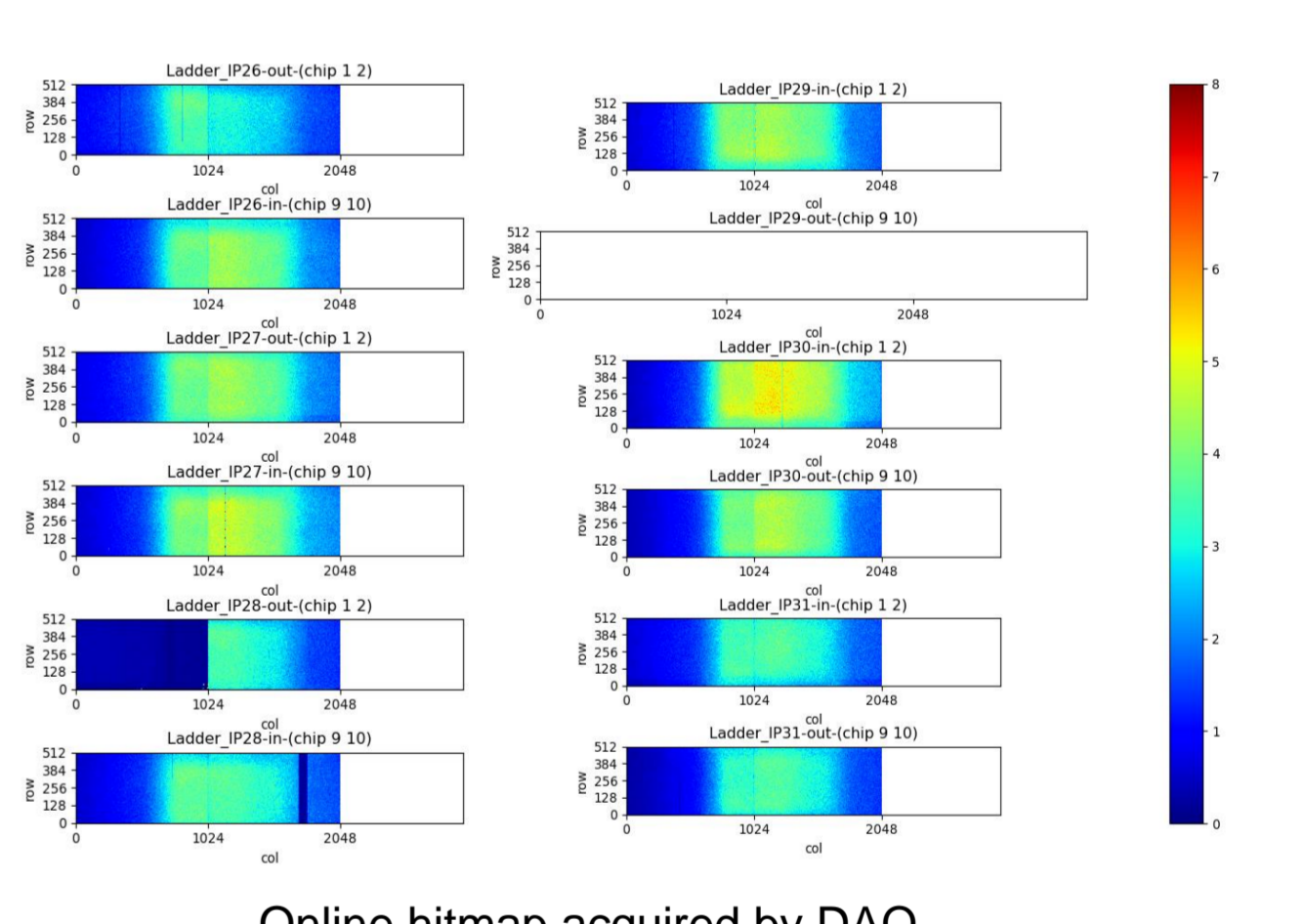
- For beam test, only one end of ladder are readout.
- TaichuPix-3 is set with triggerless mode
- The peaking data rate to DAQ system is about 18 MB/s



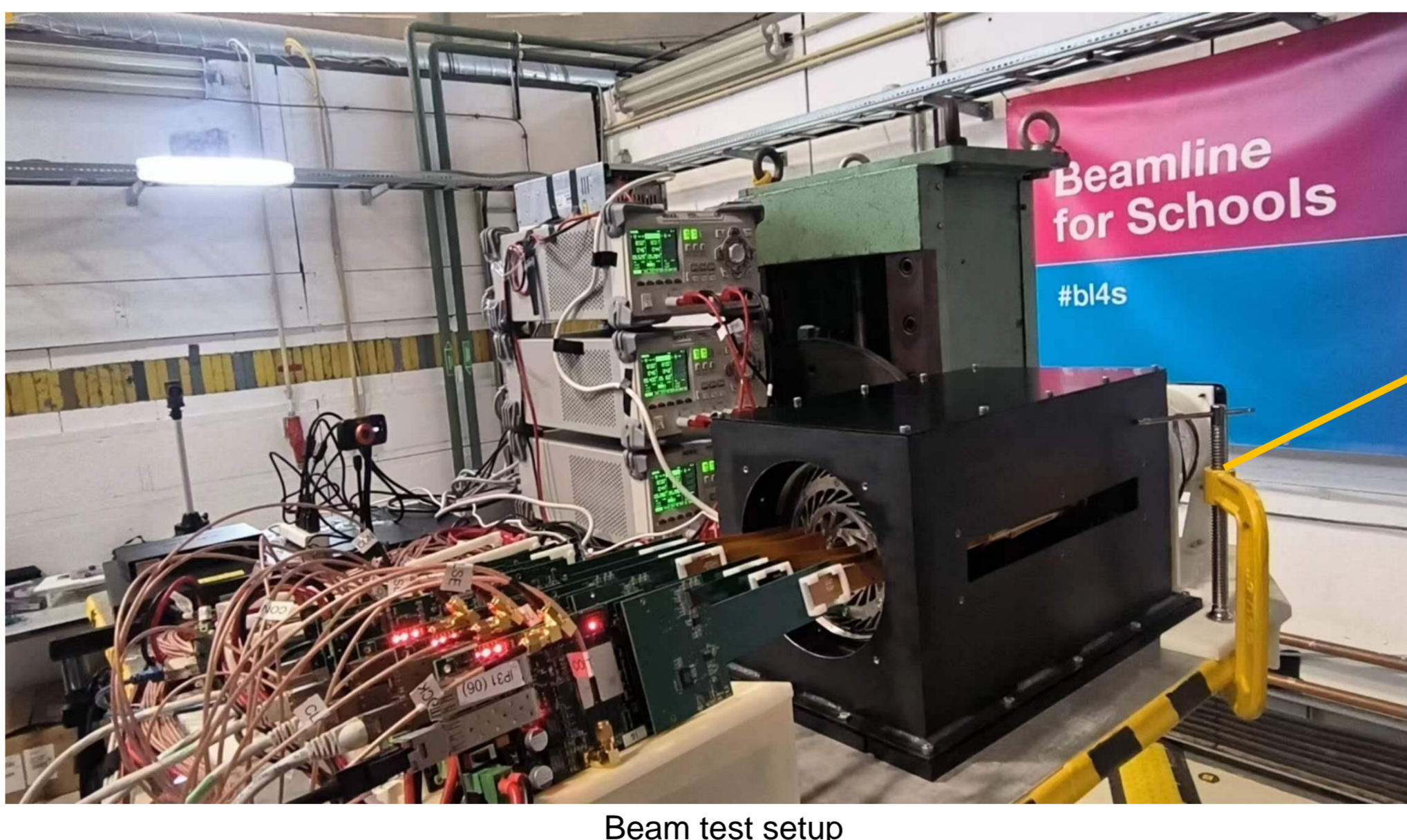
Encoding process for each data acquisition

- valid: data available flag, "1" valid, "0" invalid
- ts_chip: timestamp from pixel array
- column: column address of the firing pixel
- row: row address of the firing pixel
- pattern: pattern for data compression
- ts_FPGA: timestamp from FPGA
- chip_ID: ID number of each TaichuPix-3

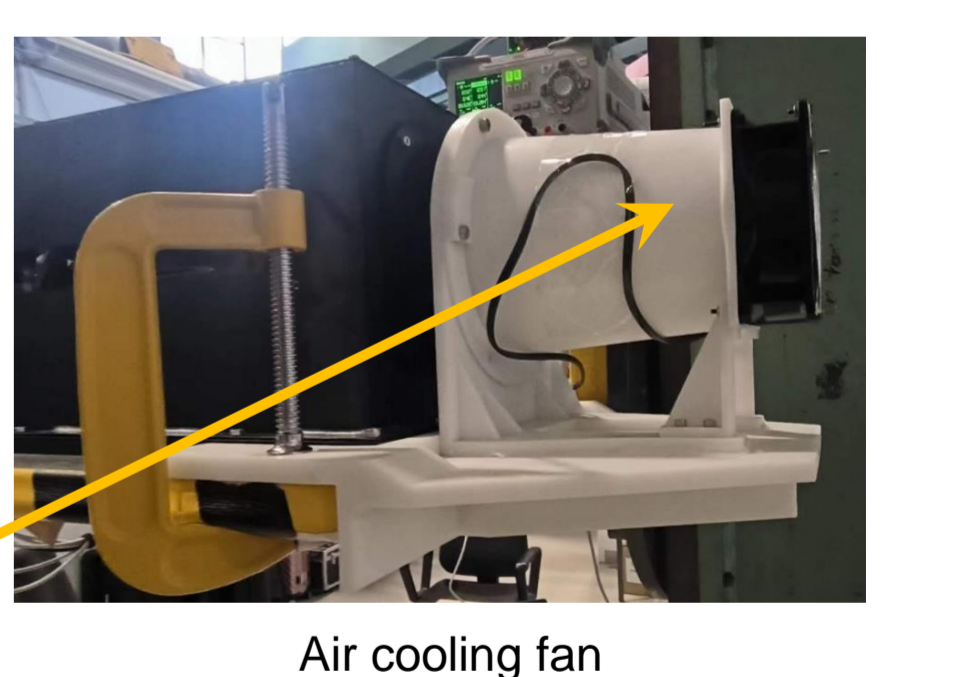
- All equipment fits in the 3D stage at DESY II TB21 hut.
- A bigger collimator ($2.5 \times 2.5 \text{ cm}^2$) is used to focus on the center of two TaichuPix-3 chips.
- Three sensors are not working correctly, and they were completely shielded.
- Threshold scan for inner layer ladder and middle layer ladder on 4 GeV, 5 GeV and 6 GeV beamline
- Operating 21 sensors together with different energies.



Online hitmap acquired by DAQ

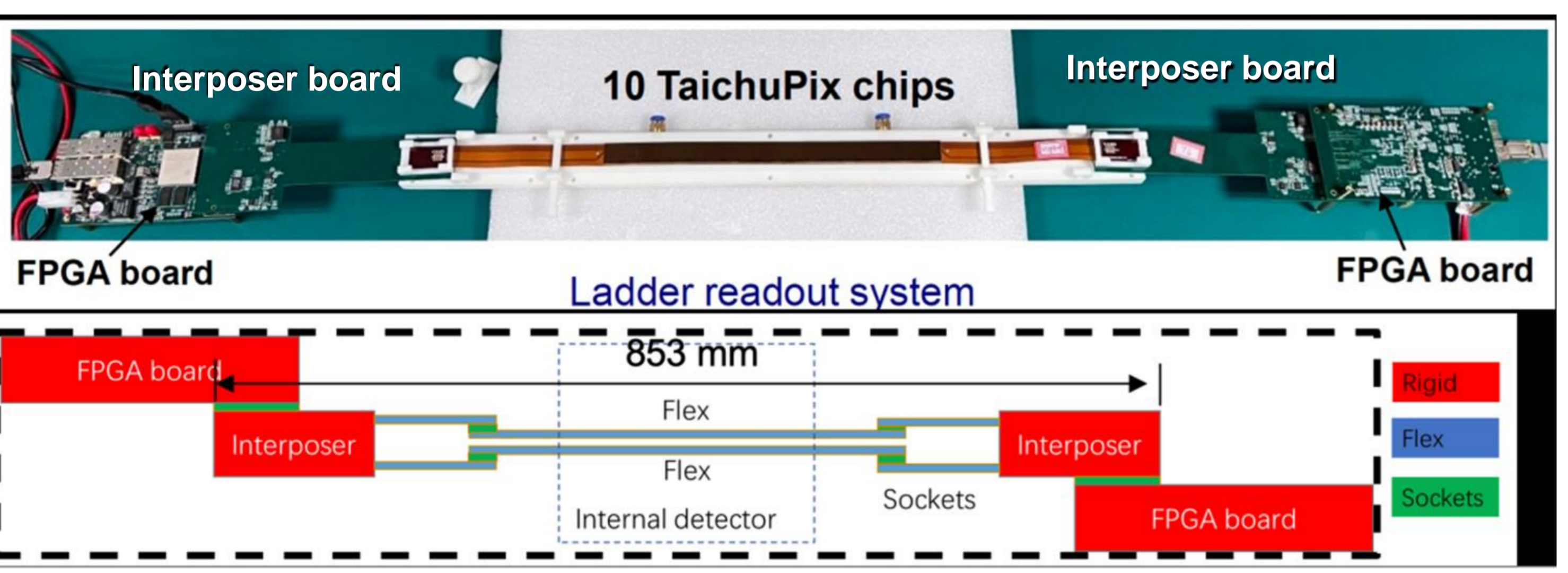


Beam test setup



Air cooling fan

The outermost layer temperature was reduced to 28°C from 40°C with the fan or dry ice.



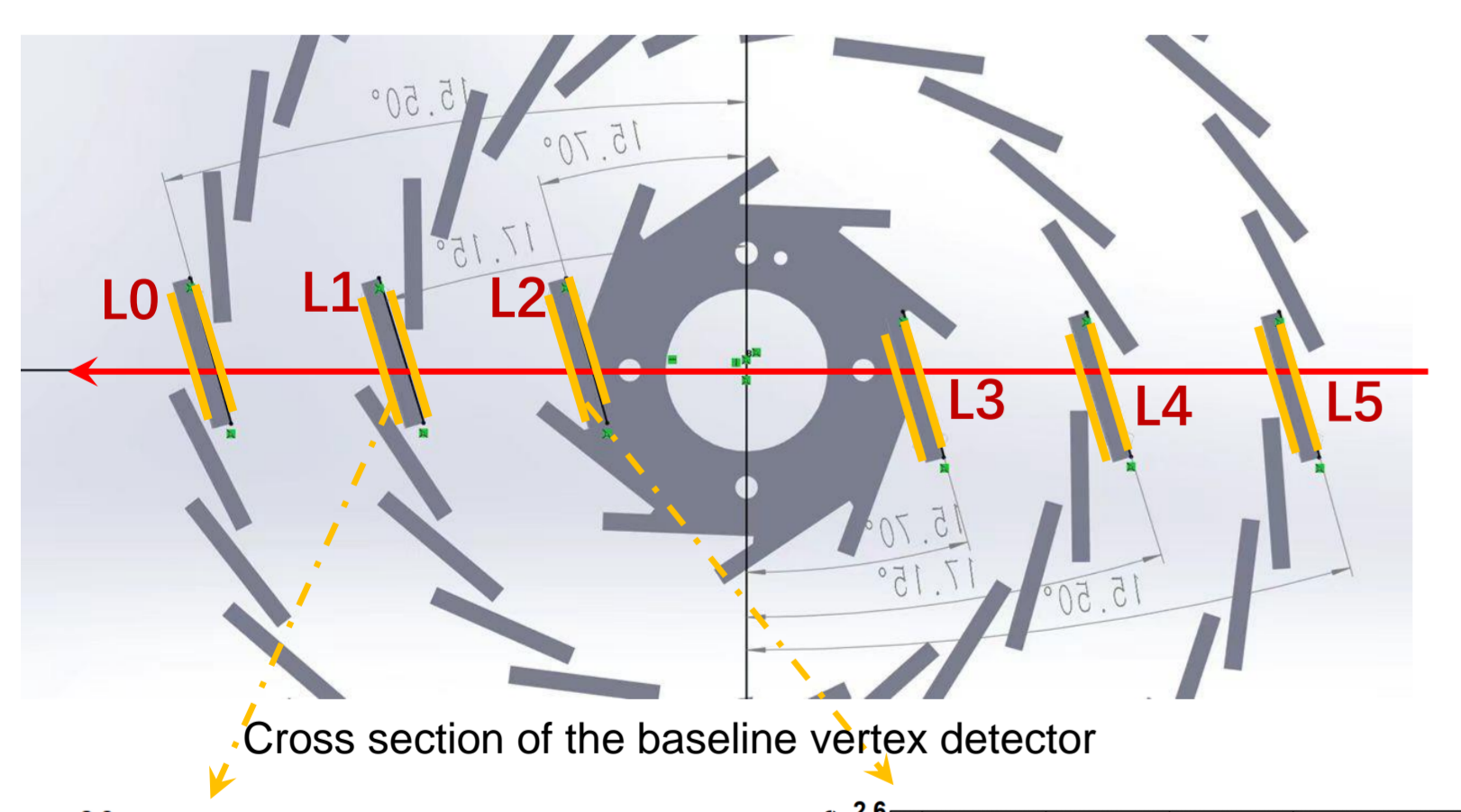
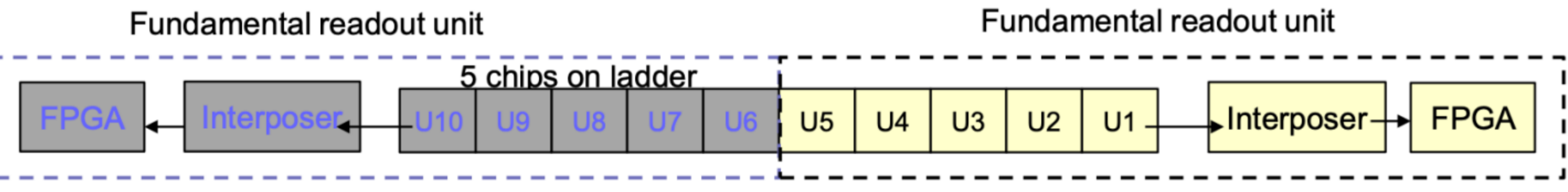
- A detector module includes 10 sensors, flexible PCB, interposer board, support structure, and a monitoring FPGA board.
- One ladder is made of two detector modules, which are glued to the front and back sides of a carbon fiber support.
- Sensors are glued and wire bonded to the flexible PCB.
- Signal, clock, control, power, ground will be handled by monitoring FPGA board through flexible PCB.

Challenge:

- Long flex cable brings some issue with power distribution and delay
- Limited space for power and ground placement

Solution: Readout from both ends, readout compose of three parts, careful design on power placement

→ A full ladder includes two identical fundamental readout units, each contains 5 TaichuPix chips, an interposer board, a FPGA readout board



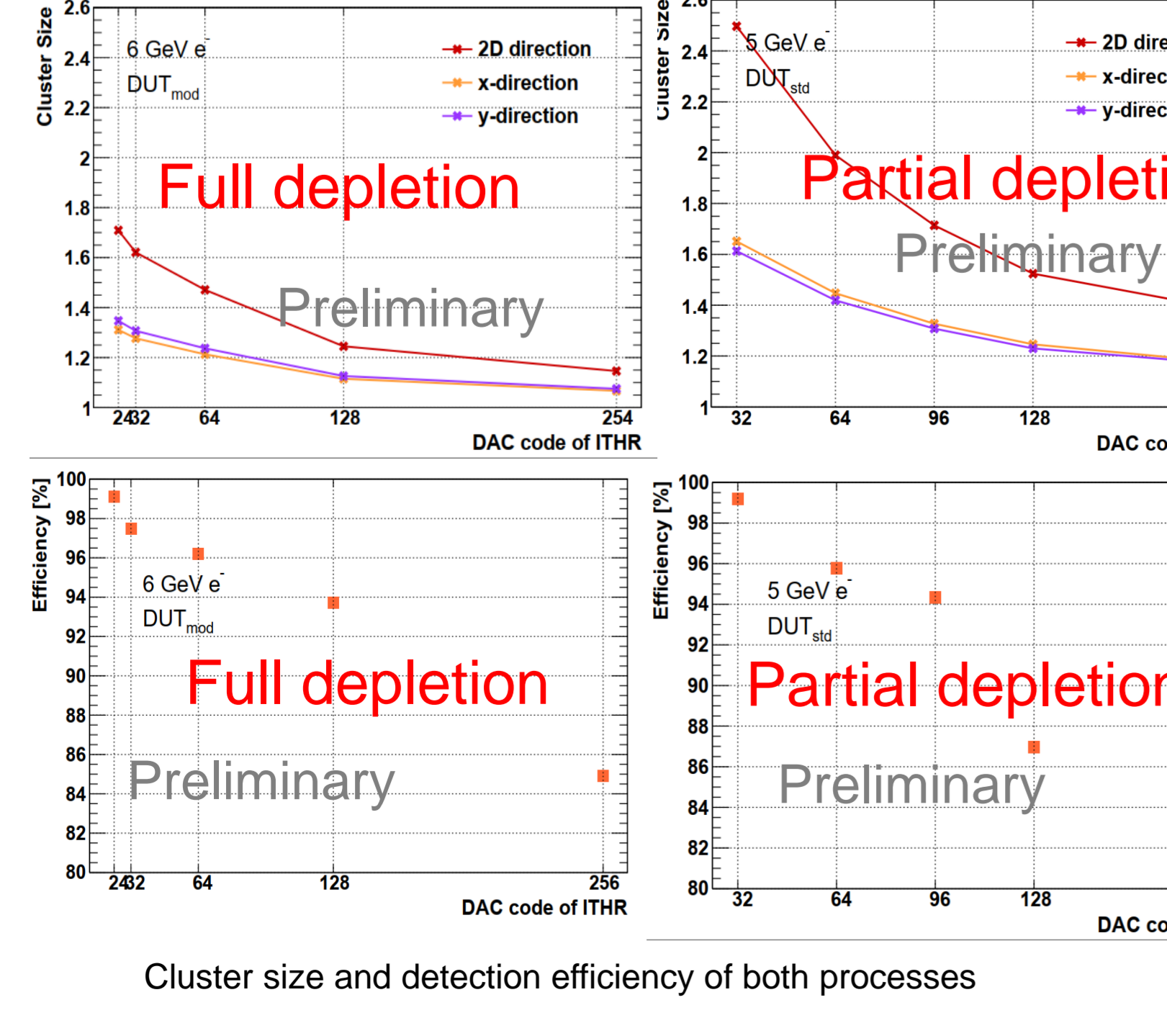
	L0-L1	L1-L2	L2-L3	L3-L4	L4-L5
Space(mm)	21.2	20.6	37.46	20.6	21.2

- Totally six ladders are assembled in the baseline vertex detector.
- The space between each ladder not the same.

- Track Reconstruction:**
- No magnetic field
 - Least squares fitting (Straight line fit)
 - No considering multi-scattering
 - Alignment is accomplished by using Millepede (c++ version) matrix method

- Cluster**
- Cluster size decreases with rising threshold.
 - Overall cluster size of full depletion is smaller.

- Detection efficiency**
- With increasing threshold, the efficiency decrease
 - Maximum eff. for DUT_{mod} is 99.1%, maximum eff. for DUT_{std} is 99.2%.



Cluster size and detection efficiency of both processes

Conclusion

- Full size TaichuPix-3 prototype is developed and tested, which shows a spatial resolution less than $5 \mu\text{m}$.
- Over 800 million valid tracks are collected during beam test.
- First CEPC silicon vertex detector prototype was realized
- Beam test results of both processes indicate a detection efficiency better than 99 %.
- More analysis is undergoing.

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