Contribution ID: **201** Type: **Poster**

Design updates for AARDVARCv4: Waveform Sampling System On Chip with Picosecond Timing Resolution

Thursday 5 October 2023 18:40 (20 minutes)

In this article we describe the measurement results on an "AARDVARC"prototype in 130 nm. AARDVARC is a multi-channel waveform digitizing and processing Application Specific Integrated Circuit (ASIC) front-end. We report on various performance metrics: fast sampling (10-14 Gsa/s), deep storage (32K samples), timing resolution (better than 5ps), low power consumption (<100mW/channel).

Summary (500 words)

State of the art large collider experiments pose conflicting requirements to the data acquisition electronics: extreme integration and density, extremely good timing accuracy, low power, high data transfer rates, large radiation awareness. The sheer number of channels also calls for reduced per-channel cost. In order to achieve accuracy goals, fast waveform sampling and digitization are often preferred to allow for tracking of radiation degradation of the light detectors, pile up events and ultra precision timing resolution.

Through higher integration with analog signal conditioning, waveform sampling, digital readout and signal processing with extended digital functions on chip, the AARDVARC allows for flexible digital signal processing within the front-end which reduces the amount of data needed to be transferred to the backend. The device performs continuous sampling and deep analog storage and on-demand or self-triggered digitization of analog storage, packetization and digital transmission (with parallel or serial interfaces). The AARDVARC v4 ASIC has been fabricated in 130nm process (in Dec 2022). In this paper we cover various measurement results from the testing campaign.

Voltage Noise/RMS: due to the distributed nature of the ADC conversion, the individual samples are subject to large recording offsets ("pedestals"), that need to be measured, recorded and corrected. The remaining errors in voltage conversion after this correction are due to noise during conversions, and have been measured for each storage sample position. The typical errors are normally distributed with a standard deviation of approximately 0.7 mV.

Sampling Speed: AARDVARC uses an internal Delay Locked Loop (DLL) to adjust and control a variable delay line - by controlling the frequency of an input clock it is therefore possible to automatically adjust the sampling frequency. The sampling speed of the AARDVARC was measured by feeding a fast periodic input (approximately 1GHz). The results for a sampling frequency of 13 GSa/s will be presented.. Effect of sampling rate on various ASIC parameters has been studied.

Accuracy/Sample jitter: To better study the achievable accuracy, the individual sample stability was investigated by feeding a signal whose phase relationship with the sampling clock was known and with jitter better than 100 fs. By varying the phase and repeating the measurement, jitter as a function of sampling array position was investigated, as it was expected that it would increase with integrated delay across the delay chain. The delay distribution for an individual sample position will be presented. Both measurements are performed at a sampling rate of 13 GSa/s. At this sampling rate, the figure shows that individual samples have a stable timing with a standard deviation of less than 2.5ps across the entire sampling space. Other experiments show that the accuracy is higher for higher sampling frequency - this is understood, and due to the specifics of

the delay line. Methods to better control jitter at lower sampling rates are now being studied and will be implemented in the next revision of the AARDVARC.

Author: Dr MOSTAFANEZHAD, Isar (Nalu Scientific, LLC)

Co-authors: CHOCK, Chris (Nalu Scientific, LLC); Mr UEHARA, Dean (Nalu Scientific, LLC); VARNER, Gary (University of Hawaii); UEHARA, Greg; MACCHIARULO, Luca; Dr PERRON, Ruth (Nalu Scientific, LLC)

Presenter: Dr MOSTAFANEZHAD, Isar (Nalu Scientific, LLC)

Session Classification: Thursday posters session

Track Classification: ASIC