DESIGN OF THE OBELIX MONOLITHIC CMOS PIXEL SENSOR FOR AN UPGRADE OF THE BELLE II VERTEX DETECTOR

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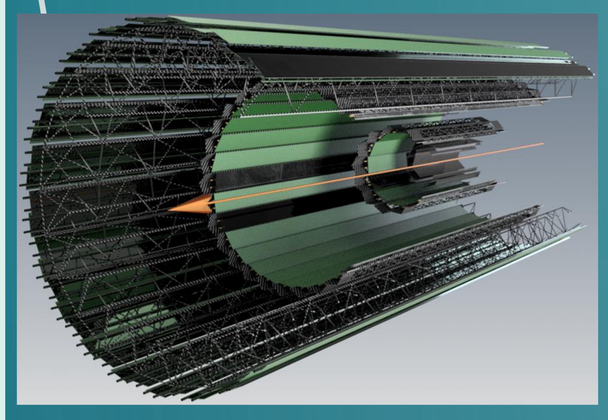
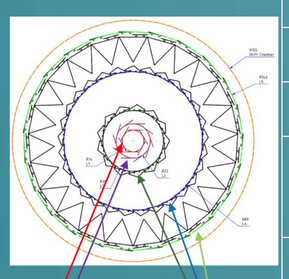
Abstract: The Belle II collaboration has initiated a program to upgrade its detector in order to address the challenges set by the increase of the SuperKEKB collider luminosity, targeting $6x10^{35}$ cm^2s^{-1}. A monolithic CMOS pixel sensor named OBELIX (Optimized BELLe II pIXel) is proposed to equip 5 detection layers upgrading the current vertex detector. Based on the existing TJ-Monopix2, OBELIX is currently designed in 180 nm CMOS process.

Belle II Vertex VTX Detector Upgrade Proposal

- Radii from 1.4cm to 14cm
- Angular acceptance 17 to 160 degrees
- ~1m² silicon surface equiped with OBELIX sensor

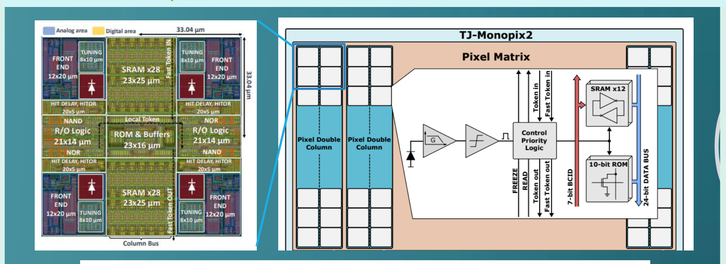


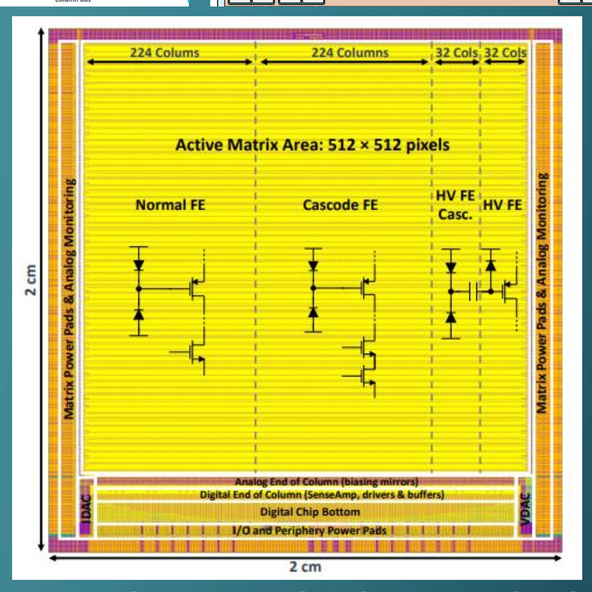


From simulations	Belle II VTX
Spatial res.	<10-15µm
Total material budget Inner-outer layers	0.1 – 0.8 %Xo
Max hit rate	120MHz/cm²
Time precision	<100ns
Trigger (freq) (delay)	30 kHz 5-10µs
Rad.hard. (TID) (fluence)	<100 kGy/year $<50x10^{12}n_{eq}cm^{-2}$/year
Power	<200mW/cm²

TJ-Monopix2 sensor

(Developed for ATLAS-ITK: doi: 10.1016/j.nima.2020.164460)





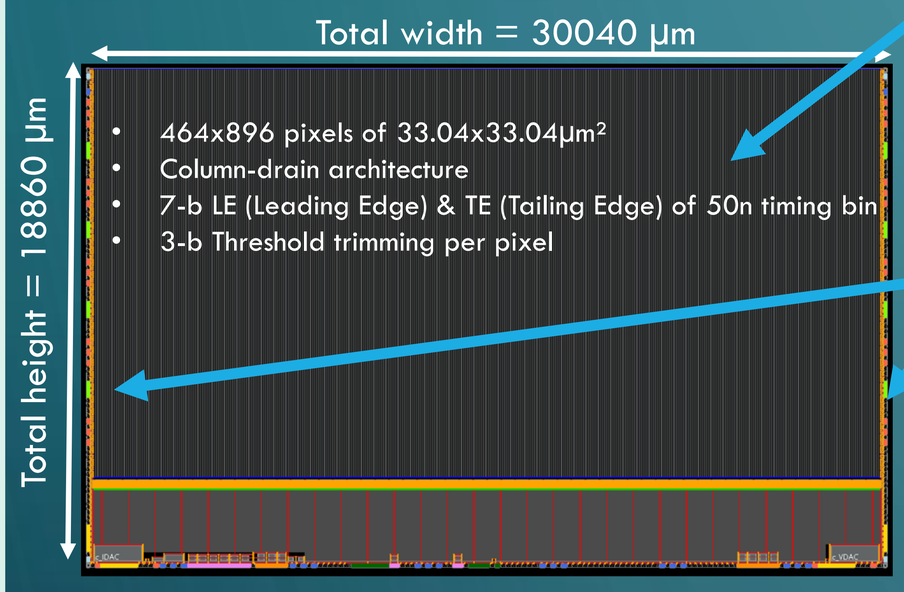
Operation demonstrated with average threshold ~200e- and threshold spread < 20e-

TJ-Monopix2 pixel performances fit Belle II VTX specifications ➔ forerunner for OBELIX

Analog & Integration

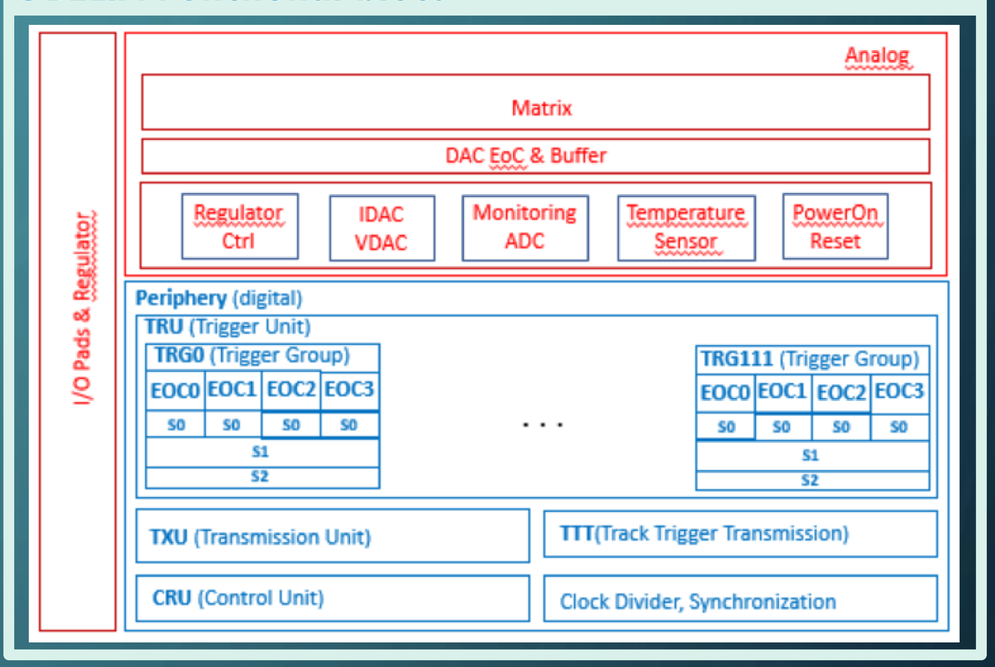
Additional analog functionalities:

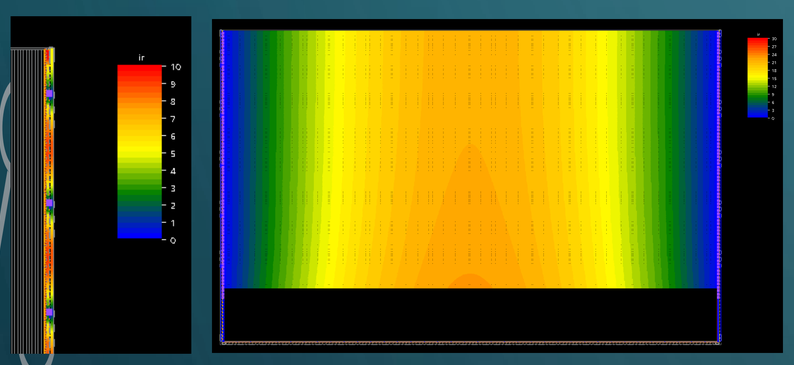
- Increase pulsing calibration pulse dynamic from ~1700e- to 2400e-
- Temperature sensor
- 10-b Monitoring ADC
- PowerOn Reset (Y. Degerli – IRFU Institut)



- Sensitive area +30%: 17x17mm² ➔ 15x25mm².
- Narrow LDO regulators (270µm) to compensate for the voltage drop on the ladder

OBELIX Functional blocs





Preminilary IR Drop estimation

Digital On Top (DoT) integration flow

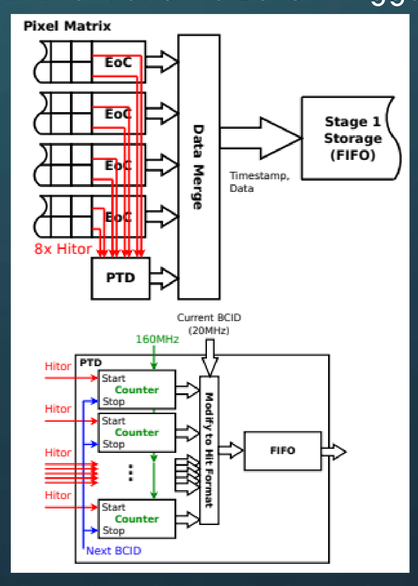
- Early power distribution analysis
- Flexible floorplan implementation & further modification

➔ Re-adaptation of matrix and DAC EoC layout from Analog On Top (AoT) flow

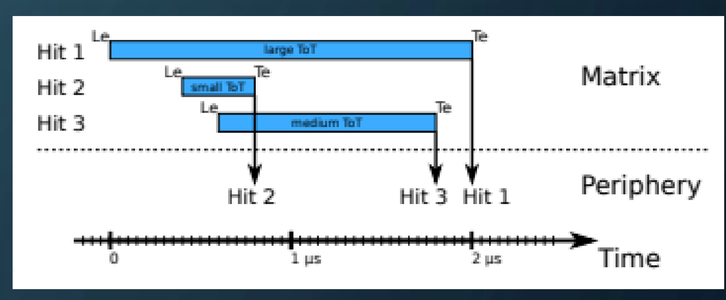
Digital functionalities

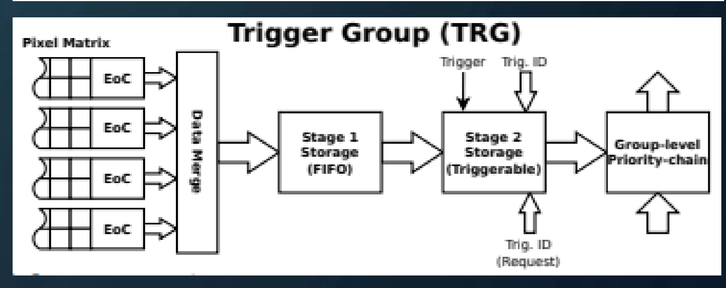
New digital functionalities:

- 2-stages trigger logic
- Peripheral Time To Digital (PTD) converter based on HitOr signal from matrix & 160MHz clock ➔ better resolution than 50ns
- Track Trigger Transmission (TTT): 2 to 8 logical macro pixel for whole matrix to provide coarse hit information to Belle-II trigger



Peripheral Time To Digital Converter





2-stages trigger logic to handle VTX trigger & disorder peripheral event arrival times

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