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Design of the OBELIX monolithic CMOS pixel sensor for an upgrade of the Belle II vertex detector

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The Belle II collaboration has initiated a program to upgrade its detector in order to address the challenges set by the increase of the SuperKEKB collider luminosity, targeting 6x1035 cm²s-1. A monolithic CMOS pixel sensor named OBELIX (Optimized BELLe II pIXel) is proposed to equip 5 detection layers upgrading the current vertex detector. Based on the existing TJ-Monopix2, OBELIX is currently designed in a CMOS 180 nm process. This new sensor introduces an extended pixel matrix, power regulators, fast hitOR information as inputs to the trigger system and a powerful readout logic matching the Belle II requirements.

Summary (500 words)

The Belle II experiment aims to collect data from the SuperKEK collider located in Japan, at very high instantaneous luminosity, up to 6e35 cm-2.s-1. Beam conditions required at such luminosities generate large and continuous rate of background particles and sets strong challenges to the vertex detector, for which Belle II has initiated an upgrade program. The VTX project proposes to use a depleted monolithic pixel sensor for this upgrade, the OBELIX chip, in order to reach excellent granularity in space (pitch below 40 µm) and time (integration below 100 ns).
The sensor occupies an area of about 19x30 mm² and includes a 464x896 pixel array with 33.04x33.04µm² pixel pitch, as well as peripheral circuitry for power regulation, bias generation, digital control and data processing. The OBELIX pixel matrix scheme remains identical to TJ-Monopix2, which was originally developed for the ATLAS inner tracker, in order to benefit from the detection performance already assessed [Bespin, 2022]. Besides the fired pixel address, the column-drain readout provides 50 ns timing precision (relaxed from the original 25 ns) with 7 bits of arrival time and 7 bits of ToT.
The main differences between OBELIX and TJ-Monopix2 lies in the chip periphery with new powering scheme and digital processing.
To reduce the non-active area and the large number of side pads dedicated to power distribution of the matrix, as well as to facilitate the power cabling to sensors, a distributed low-dropout regulator is implemented, requiring only 5 groups of power pads per matrix side.
The new digital processing consists of four parts: Trigger Logic Unit (TLU), Transmission Unit (TXU), Synchronisation unit (SCU) and Control Unit (CTU). The TLU implementation allows to handle a maximum hit rate of 120MHz/cm² with a 30 kHz trigger rate and 10µs trigger latency. Data from 4 double columns are merged via a round-robin arbiter before being sent to a two-stage buffer. The first stage of the buffer is a FIFO and acts as a pre-memory whose size allows it to hold the event information between two triggers. The second stage is the main trigger memory, where its logic allows to associate hit data and trigger information before sending them to the TXU. The TXU frames the data with 8b/10b encoding and sends it to the 320MHz serial LVDS output. The SCU and CTU inherit from the TJ-Monopix2 design. They conform to the RD53 interface and guaranty the control and configuration of different sensor parameters.
The overall chip is designed so that the power consumption is less than 200 mW/cm² at an average 60 MHz hit rate and with 50 ns time-stamping.
This presentation will review the overall design of the OBELIX sensor, which is scheduled for submission in Q4 2023. We will specifically focus on the new features introduced over the TJ-Monopix2 prototype and on the design methodology approaching digital-on-top flow..

Bespin, C. (2022). Charge collection and efficiency measurements of the TJ-Monopix2 DMAPS in 180 nm

CMOS technology. Pixel2022. Santa Fe, New Mexico, USA: Proceeding of Science.

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