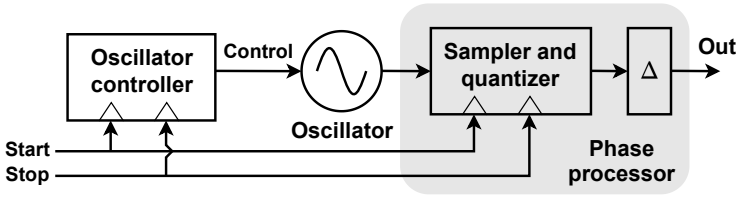

Figure 1: General structure of an oscillator-based TDC.

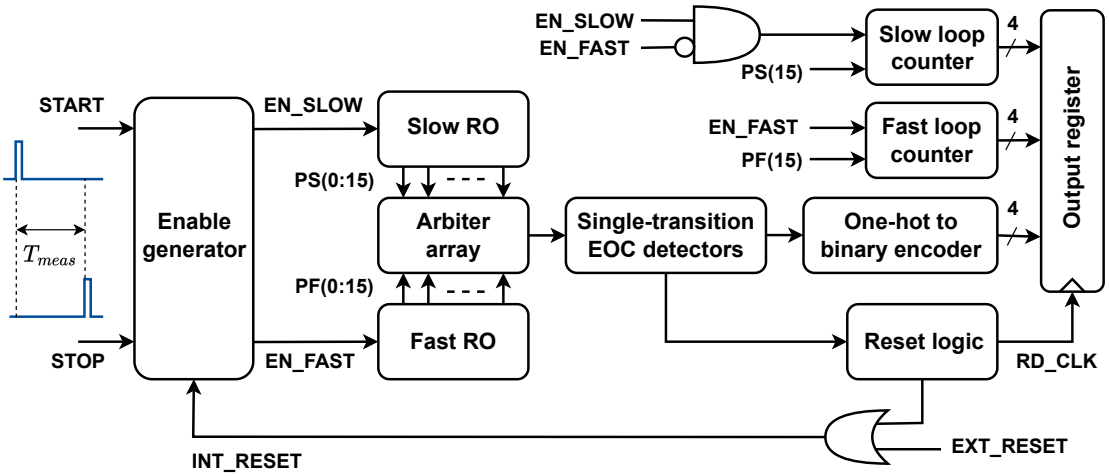

Figure 2: Block diagram of the proposed gated Vernier ring oscillator (GVRO) TDC.

Table 1: Simulated performance of the proposed GVRO TDC at different temperatures. Values refer to a supply voltage of 1.2V unless mentioned otherwise.

Parameter	**Value at 300K**	**Value at 77K**
Timing resolution (LSB)	9.5 ps	4.9 ps at 1.2V 6.2 ps at 1.0V
Dynamic range (DR)	40.2 ns (12 bits)	29.4 ns (12 bits)
Maximum conversion time	38 ns	28 ns
Active power consumption	0.73-1.9 mA at 1.2V	0.88-2.2 mA at 1.2V 0.50-1.1 mA at 1.0V