# A Low-Power Gated-Vernier Ring Oscillator TDC for Cryogenic Detectors

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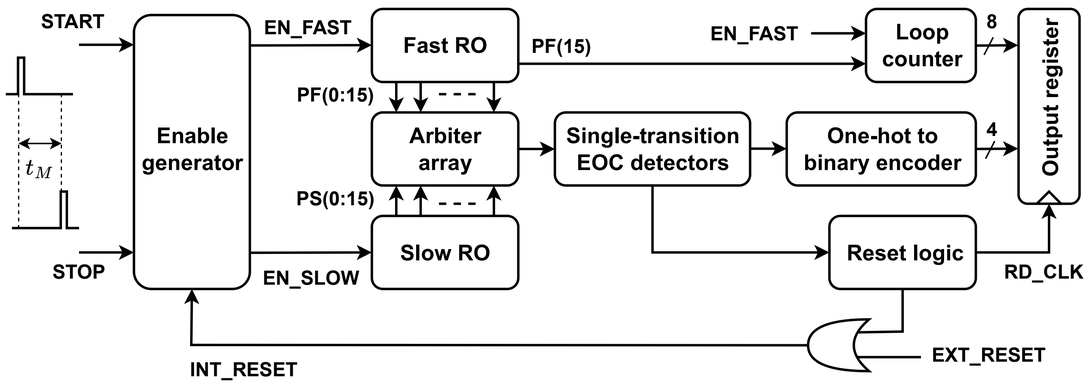
## Abstract

High-resolution time-to-digital converters (TDCs) are required for time-of-flight measurements in many scientific applications, including particle identification for high energy physics, biomedical imaging methods such as PET, and associated particle imaging (API). FPGA-based TDCs are popular for such applications but suffer from limited resolution and high power consumption compared to custom ASICs. In addition, full-custom TDC designs can be integrated within the signal chain of multi-channel or pixelated front-end ASICs, thus eliminating the need for power-hungry low-latency links to external FPGAs. Several applications for such fully-integrated TDCs, such as photon time stamping in rare-event search experiments, also require cooled detectors and front-end electronics. Here we describe a full-custom TDC in 90nm CMOS technology designed for high-resolution and low-power operation in such cryogenic environments.

## Overall TDC architecture



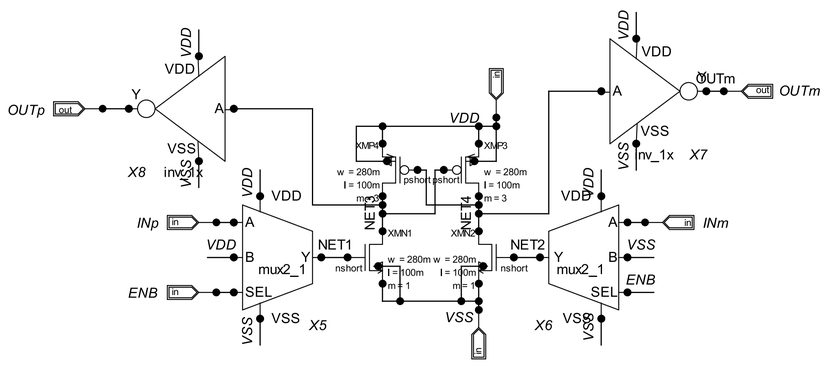

- Gated Vernier ring oscillator (RO) architecture.
- Power reduced using single-transition end-of-conversion (EOC) detectors.
- Effective time resolution is set by the delay difference between slow and fast RO stages, $\Delta = T_s - T_f$, as for basic Vernier TDCs.
- The differential delay, Δ, (i.e., the LSB of the TDC) has first-order robustness to PVT variations if the two ROs use matched circuits.
- The use of ROs (instead of open-loop delay lines) reduces the number of stages required to cover a given delay range, i.e., increases the dynamic range (DR).
- Gating the RO on/off preserves phase, thus providing first-order noise shaping of quantization errors in periodic applications (such as all-digital PLLs).

## Circuit design

- The design was implemented in the Skywater S90 ROIC 90nm CMOS process:
  - 7 metal layers, MIM capacitors, TSVs, stitching support.
  - Default ”military” device models are rated from -55C to +125C, cryogenic models are available at 45 K, 77 K, 120 K, and 150 K.

### Differential delay cell

- Cross-coupled PMOS pair provides positive feedback to ensure rail-to-rail swings.
- Input multiplexers allow the oscillator to be gated on/off by the start or stop signal.
- Strength of the buffer inverters is increased to add extra delay (used in the slow RO).

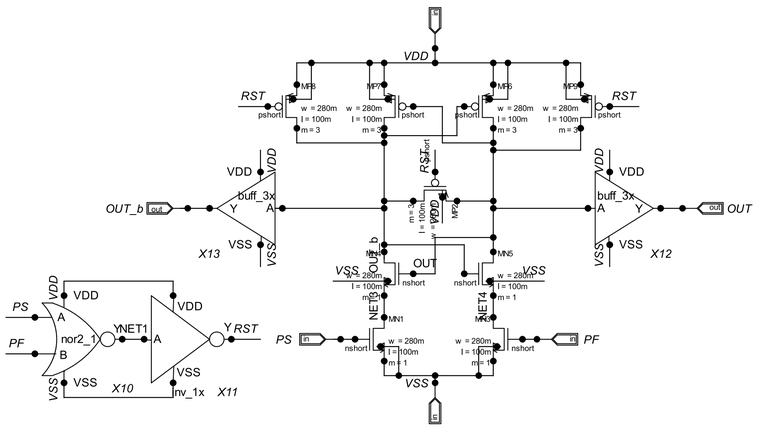



### Arbiter

- Acts as a time comparator, i.e., detects whether the fast RO edges (PF) are ahead or behind the slow RO edges (PS):

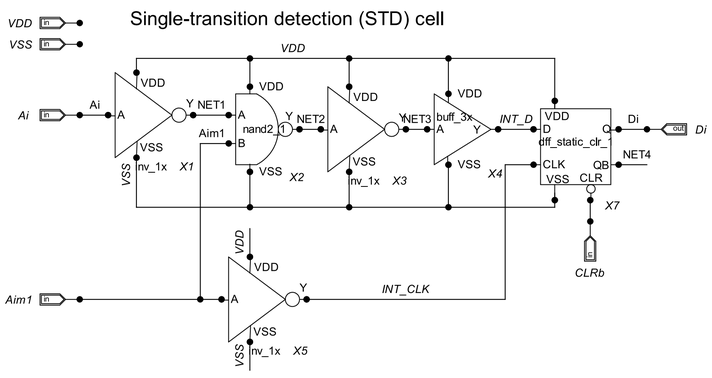
$$Out(i) = \begin{cases} 1, & \text{if } PF(i) \text{ is behind } PS(i) \\ 0, & \text{if } PF(i) \text{ is ahead of } PS(i) \end{cases}$$

- Simpler and lower power than using a D-type flip-flop (DFF).
- A DFF (not shown) is used to sample the output of the arbiter at rising edges of the fast RO, i.e., PF(i).
- Dummy clock path delays ensure setup time of the DFF is not violated.



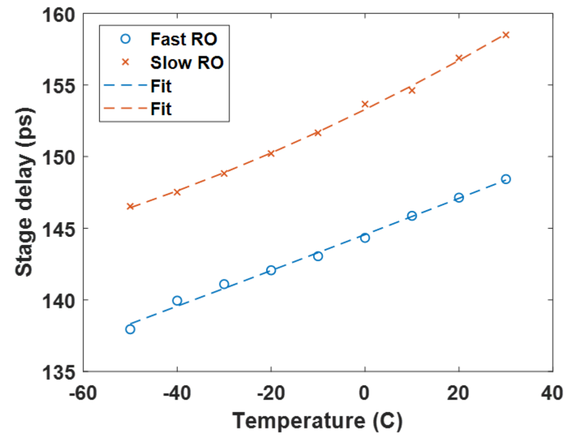

### Single-transition EOC detector

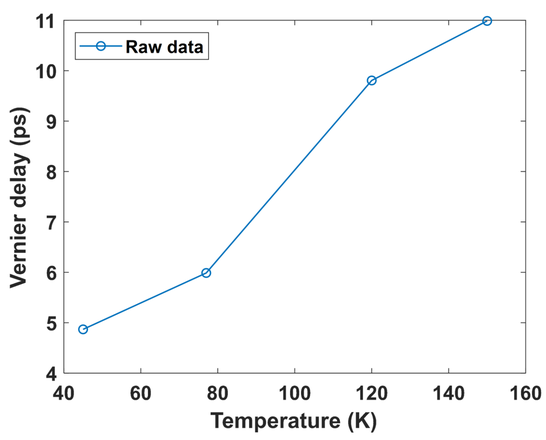
- Reduces power consumption by ensuring that only one transition is generated per conversion.
- Detects falling edges in the sampler outputs, A(i), which correspond to an edge coincidence and thus the end of conversion (EOC).
  - D(i) = 1 only if A(i-1) = ‘1’ and A(i) = ‘0’.
- Data path delay of the DFF is longer than the clock path delay to ensure that the previous value of INT_D is sampled without any timing violations.



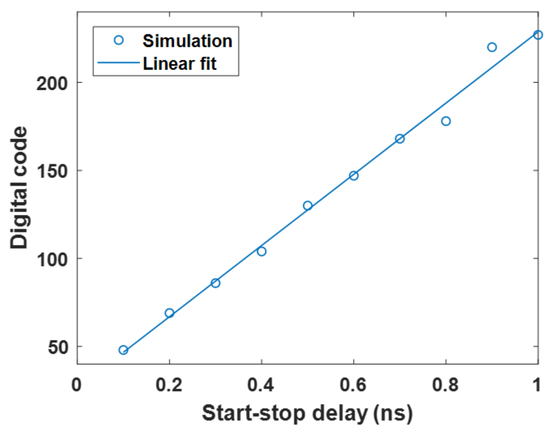

## Cryogenic simulation results

- Characterization of delay cells at cryogenic temperatures

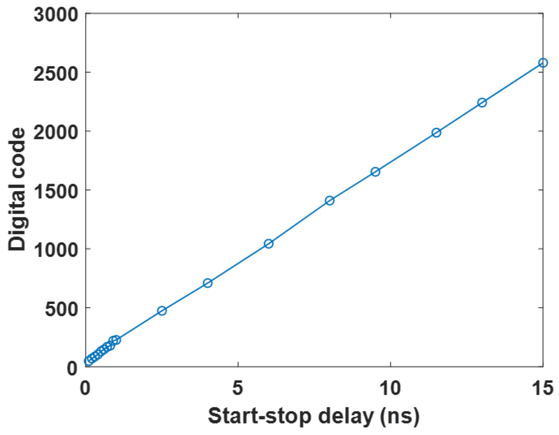



- Full TDC simulations (at 77K, tt corner)
  - Maximum conversion time = $16T_f \approx 28$ ns.
  - Active power: 0.88 mA (before STOP), 2.2 mA (after STOP) → 10% larger than at 300K
  - Quiescent power: 30 nA @1.2V → 1000x less leakage at 77K (4x higher subthreshold slope)

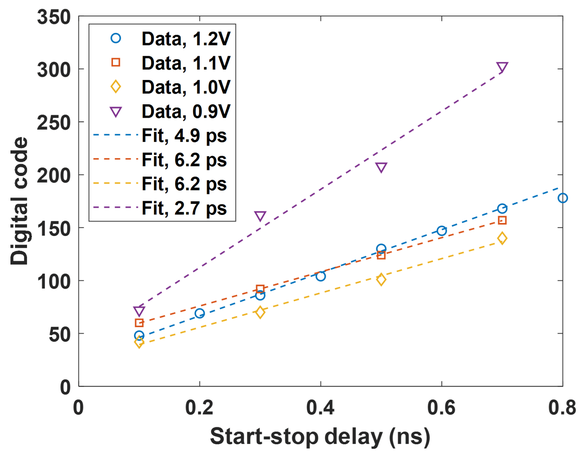



$N_s$ = 0, 8-bit resolution

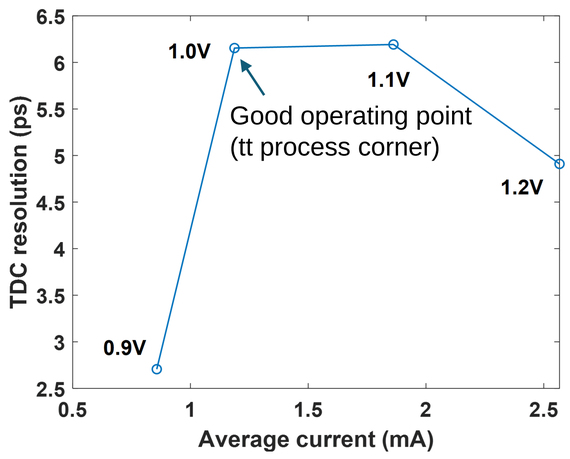



$N_s \geq 0$, 12-bit resolution

- The power supply voltage of the TDC can be adjusted to optimize the trade-off between resolution and power consumption.




Effect of $V_{DD}$ on resolution at 77K




Power-resolution trade-off at 77K

## Performance summary

| Parameter | Value @300K | Value @77K |
|---|---|---|
| Timing resolution (LSB) | 9.5 ps | 4.9 ps @1.2V<br>6.2 ps @ 1.0V |
| Dynamic range (DR) | 40.2 ns (12 bits) | 29.4 ns (12 bits) @1.2V |
| Maximum conversion time | 38 ns | 28 ns |
| Active power consumption | 0.73-1.9 mA @1.2V | 0.88-2.2 mA @1.2V<br>0.50-1.1 mA @1.0V |

- Nominal supply voltage: 1.2V, can be reduced to 1.0V
- The proposed TDC design has good resolution (5-6 ns) and high DR (~30 ns) with relatively low power consumption (<1.1 mW at 1.0V).
- Layout area is expected to be small since the two ROs use a combined total of only 16 delay stages.
- Post-fabrication linearity (as quantified by INL and DNL) can be improved by using code density tests to populate a lookup table (LUT).

## Conclusions

Key design requirements for cryogenic TDCs include high resolution, wide DR, low power consumption (to minimize cryogen loss rates), and minimal hardware usage. The proposed design uses gated Vernier Ros to improve the trade-off between these parameters relative to conventional delay-line based flash TDCs.

## References

[1] Cheng, Zeng, M. Jamal Deen, and Hao Peng. "A low-power gateable Vernier ring oscillator time-to-digital converter for biomedical imaging applications." *IEEE Transactions on Biomedical Circuits and Systems* 10.2 (2015): 445-454.

[2] Yu, Jianjun, Fa Foster Dai, and Richard C. Jaeger. "A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13µm CMOS Technology." *IEEE Journal of Solid-State Circuits* 45.4 (2010): 830-842.

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