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A Low-Power Gated-Vernier Ring Oscillator TDC for Cryogenic Detectors

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High-resolution time-to-digital converters (TDCs) are required for time-of-flight measurements in many applications, including particle identification for high-energy physics. FPGA-based TDCs are popular for such applications but suffer from limited resolution and high power consumption compared to custom ASICs. Full-custom TDC designs can also be integrated within multi-channel or pixelated front-end ASICs, thus eliminating power-hungry low-latency links to external FPGAs. Several applications for such integrated TDCs, such as photon time stamping in rare-event searches, also require cooled detectors and front-end electronics. Here we describe a full-custom TDC in 90nm CMOS technology designed for high-resolution and low-power operation in such cryogenic environments.

Summary (500 words)

Key requirements for a cryogenic TDC include high resolution, wide dynamic range (DR), low power consumption, and minimal hardware usage. The proposed design uses ring oscillators (ROs) to improve the trade-off between these parameters relative to delay-line based flash TDCs. Specifically, the number of open-loop delay stages required for a full-scale range of Tmax is given by N = Tmax/Δ, where Δ is the resolution. By contrast, RO-based TDCs have unlimited DR since the "start" signal continuously circulates through a set of delay stages. Fig. 1 shows a generic model for an oscillator-based TDC. The oscillator is switched between two operating modes, with the control signal being generated by a logic circuit (the oscillator controller) based on the "start" and "stop" signals. A phase processor uses an array of arbiters to sample the oscillator output, thus generating the TDC output code.

The resolution of RO-based TDC architectures can be improved by using the Vernier principle. Here we describe a 12-bit gated Vernier RO (GVRO) that combines high resolution with large DR, small layout area, and low power consumption. The time difference, Tmeas, is quantized by comparing the multi-phase signals generated by slow and fast ROs that are triggered to start oscillating at the rising edges of "start" and "stop", respectively. The slow RO acquires extra phase during the Tmeas interval, so the time required for the fast RO to catch up with it becomes proportional to Tmeas. An arbiter detects this coincidence event, and Tmeas is quantized by counting the number of RO edges that have elapsed until the arbiter changes state.

Fig. 2 shows a block diagram of the proposed GVRO TDC, which uses the SkyWater S90 90nm bulk CMOS process and was simulated using cryogenic device models (45-150K). The design uses 1) fully-differential 8-stage ROs; 2) dynamic TSPC flip-flops to minimize propagation delays; 3) custom dynamic latches as arbiters; and 4) single-transition end-of-conversion (EOC) detectors to minimize the number of logic transitions during each conversion. The 4-bit output of the EOC detectors provides a thermometer-coded version of the LSB outputs. The next 4 bits are generated by counting cycles of the fast RO after the "stop" signal has been detected. Finally, the 4 MSB bits are generated by counting cycles of the slow RO during the Tmeas interval.

The simulated performance of the TDC at 300K and 77K is summarized in Table 1. The proposed design has good resolution (5-6ps) and high DR (30ns, can be extended) with low power consumption (<1.1mW at 1.0V). Chip layout area is also expected to be small since the two ROs use a combined total of only 16 delay stages. Post-fabrication linearity (as quantified by INL and DNL) will be improved via digital correction of the raw TDC output, i.e., populating an on-chip lookup table (LUT) during foreground calibration by using the statistical code density test (CDT) method.

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