Fig. 1. Layout of 3FI65P1 chip
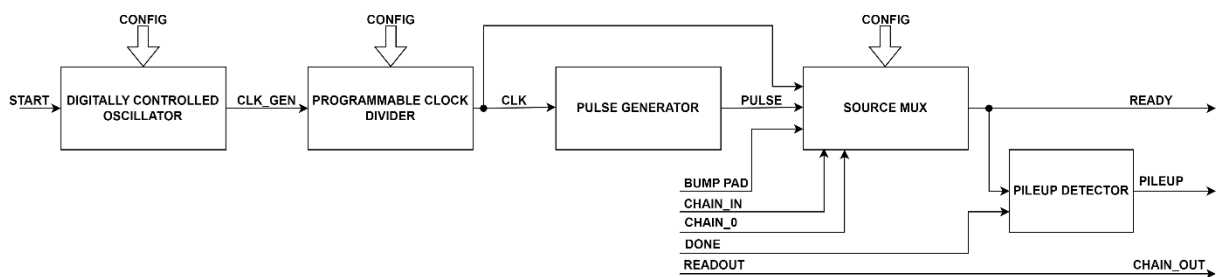

Fig. 2. Block diagram of digital circuitry implemented in the second prototype

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