# Integration of EDWARD readout architecture in full-field fluorescence imaging detector

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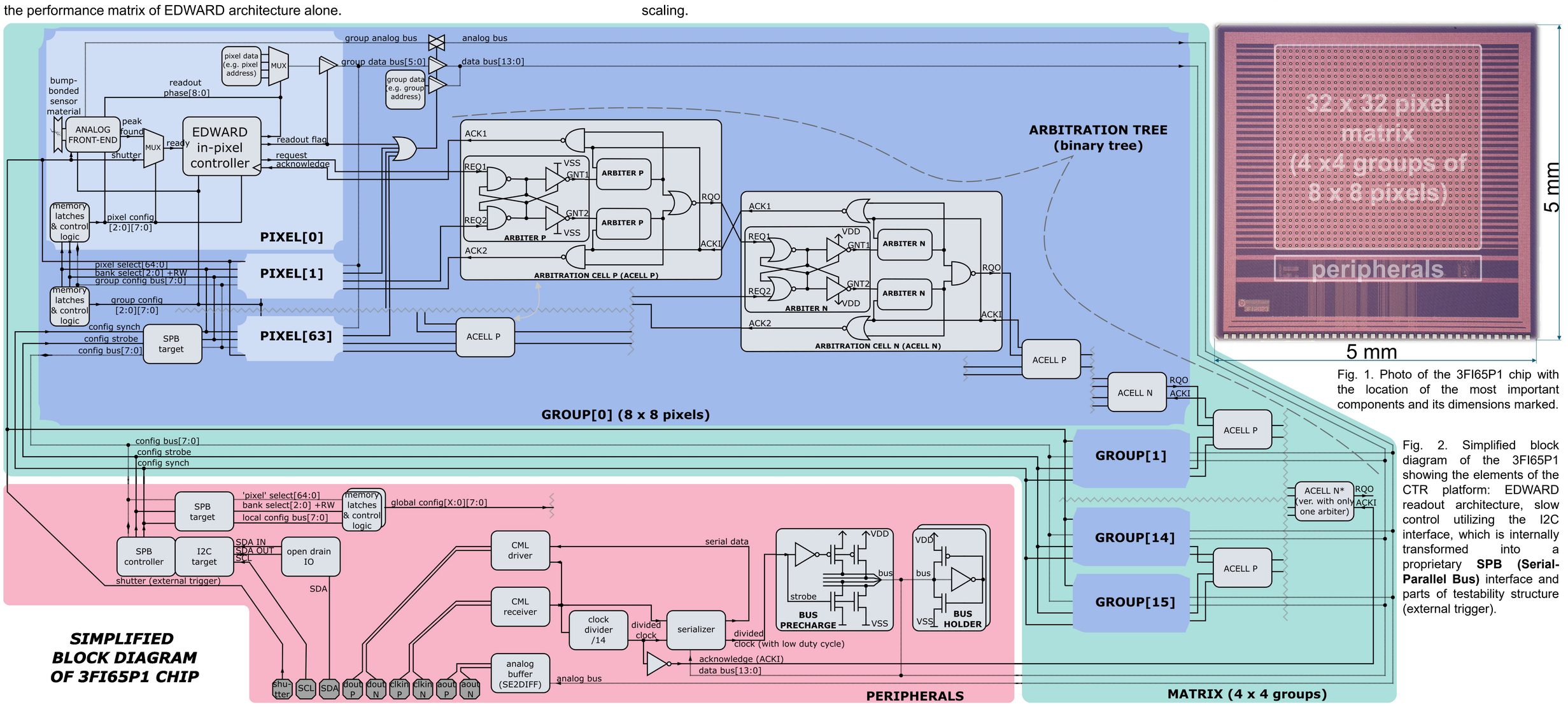
## INTRODUCTION

Data bandwidth, timing resolution and resource utilization in readouts of radiation detectors are a constant challenge. Event driven solutions are pushing against well-trenched framed solutions. The idea for an asynchronous readout architecture called **EDWARD (Event-Driven With Access and Reset Decoder)** was presented at the TWEPP 2021 conference. Here we show the progress of our work which resulted in two chip prototypes. The first one, named 3FI65P1, showed in **Fig.1**, is a full device with the analog pixel circuitry suited for full-field fluorescence imaging. It is already manufactured, and preliminary results are presented. The second chip, named EDWARD65P1, contains digital pulse generators with Poisson-exponential distribution in each pixel for extraction of the performance matrix of EDWARD architecture alone.

## READOUT ARCHITECTURE

The EDWARD readout architecture [1][2], allows efficient readout of data from a chip with multiple data sources, such as pixelated detectors. The architecture is distinguished by working in a fully asynchronous manner, meaning the request for readout can occur at any time, and the arbitration between requests is devoid of priority. These features eliminate the need to use the frame clock to snapshot the state of the matrix, which would be necessary to avoid switching between channels during a readout [3]. This functionality of the EDWARD architecture is achieved thanks to arbitration based on a binary tree, the basic unit of which is an arbiter based on the Seitz arbiter structure [4]. Other advantage of the EDWARD architecture is automatic synchronization to an external clock provided, for example, by an acquisition module, which allows the chip to send data out using a standard communication protocol. The described architecture has been incorporated into the **CTR (Configuration, Testability, Readout)** platform and implemented in two different chip prototypes in a **65nm CMOS process**. The platform, shown in **Fig.2**, is extremely modular and allows for easy scaling.




***SIMPLIFIED BLOCK DIAGRAM OF 3FI65P1 CHIP***




Fig. 1. Photo of the 3FI65P1 chip with the location of the most important components and its dimensions marked.

Fig. 2. Simplified block diagram of the 3FI65P1 showing the elements of the CTR platform: EDWARD readout architecture, slow control utilizing the I2C interface, which is internally transformed into a proprietary **SPB (Serial-Parallel Bus)** interface and parts of testability structure (external trigger).

## 3FI65P1 CHIP

The 3FI65P1 chip is suited for full-field fluorescence imaging [5]. It is a hybrid 5mm x 5mm detector containing a 32x32 pixel matrix with the 100um pitch. The matrix is built in a modular fashion with 16 groups (4x4), each consisting of 64 pixels (8x8). A digital part was synthesized and implemented with the help of CAD tools and placed between analog islands in a group, as well as between groups in the matrix. The main elements of the CTR platform are located in the group logic space (density ~84%), while the space between groups mainly contains a part of the arbitration tree between groups (density ~2%) and a shared bus. All groups are connected to the shared 14-bit digital data bus, on which addresses of pixels being read out are sent, and 1 analog line, on which analog values of the peak from a front-end peak detector are sent. The digital data is serialized and sent off-chip. Serialization is performed based on an externally supplied clock with a designed frequency of 250MHz. The chip has a built-in clock divider of 14, which acts as a serializer frame clock and determines time intervals for channel access to shared resources. This gives pixel **data readout rate of 17.86MHz**.

## EDWARD65P1 CHIP

The EDWARD65P1 prototype is based on the skeleton of the 3FI65P1, maintaining its dimensions. In this prototype the analog front-end circuitry is replaced by logic, which block diagram is depicted in **Fig.3**. It contains pulse generator with Poisson-exponential distribution [5]. This structure allows even better study of the temporal properties of the EDWARD architecture – timing resolution, delay, maximum acceptable rate, and the signal integrity of the received data thanks to the ability to programmatically change the rate at which readout requests are generated. Simulation results for such an event generator are shown in **Fig. 4**. It shows the effect of the event generation rate on the readout delay, defined as the time from the readout request to the latching of the event information in the peripheral part of the system. The delay is illustrated in the form of histograms:

- When only one pixel is active (Fig. 4a), the readout delay has a uniform distribution,
- When the generation rate is relatively low (compared to the readout rate) (Fig. 4b), the data is read out from the pixel with the first active acknowledgement generated, but sometimes the pixel has to wait for servicing of other requesting pixels,
- When the token generation rate increases (Fig. 4c), the average readout delay increases due to more pixels simultaneously waiting to be read out,
- In the extreme case (Fig. 4d), the readout delay seeks a limit equal to the frame readout i.e., each pixel must wait for all other pixels to read.

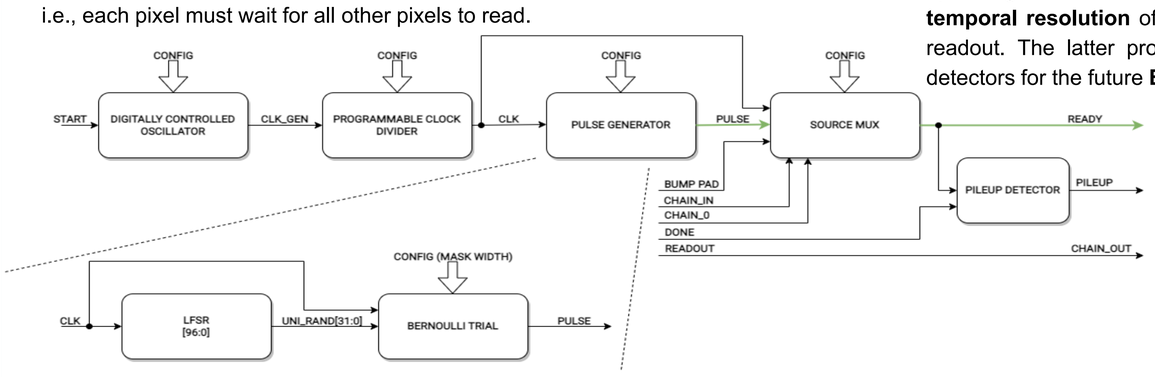



Fig. 3. Block diagram for the signal generator implemented in the EDWARD65P1 chip

## TESTING

The digital portion of the 3FI65P1 chip was tested to verify the functionality of the CTR platform. The test involved configuring the chip, triggering the readout of pixels using an external trigger, reading the serial data from the acquisition system, and repeating the steps several times, each time with the new configuration. For this purpose, each pixel was assigned a predetermined non-zero value stored in software with a maximum value of 255. The assigned value for each pixel is shown as an intensity map in **Fig. 5a**. Before each trigger, the software stored value was decremented, and the zero-value pixel was disabled. A sample I2C command to change the configuration was captured with an oscilloscope and is shown in **Fig. 6**. The test allows **all elements of the CTR platform to be tested** - sending configurations, testing with an external trigger, and checking data integrity. The resulting number of reads from all pixels is shown in the form of an intensity map in **Fig. 5b**. **Both numbers are the same for all pixels - there is no data loss or unexpected readouts.**

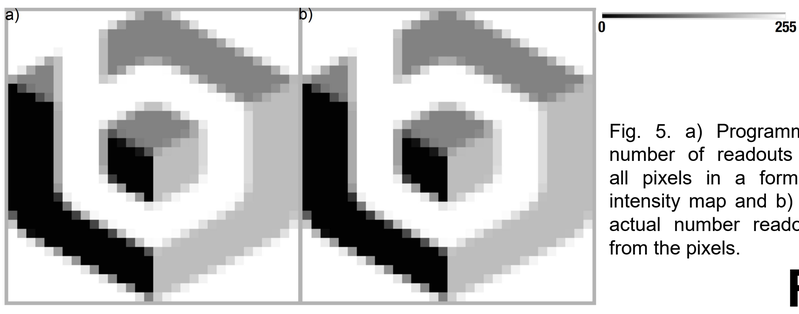



Fig. 5. a) Programmed number of readouts for all pixels in a form of intensity map and b) the actual number readouts from the pixels.

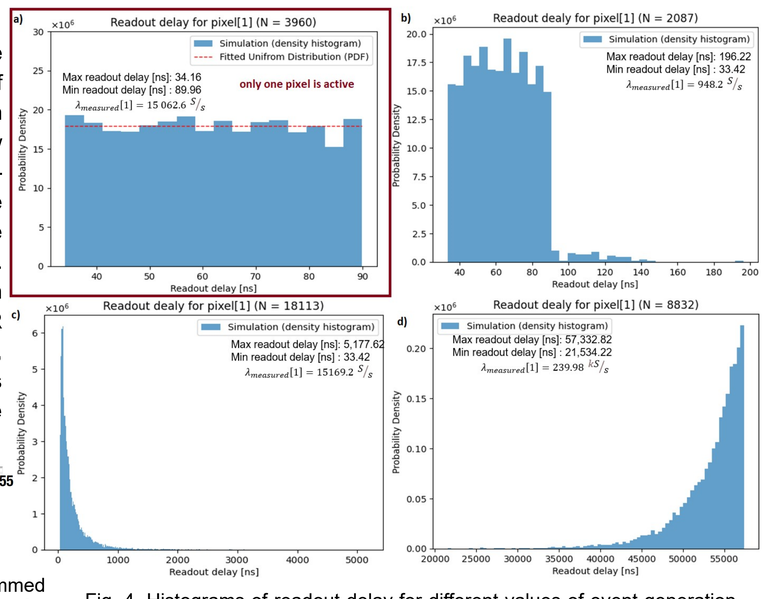



Fig. 4. Histograms of readout delay for different values of event generation rates (a) when only one pixel generates events (b) the generation rate is low compared to the readout clock frequency (~17.86 MHz) (c) the generation rate is comparable to the readout clock frequency (d) the generation rate is high compared to the readout clock frequency

## SUMMARY

The results showed here – both the simulations for the EDWARD65P1 chip and the **measurements** for the 3FI65P1 chip, **confirm the operation of the designed readout architecture** and allow to determine the timing parameters depending on the event generation rate. Use of the proposed architecture in the next generation of chips will allow not only to **reduce power consumption** by operating on the basis of **event driven**, but also to obtain much **higher temporal resolution** of the received data by getting rid of the need for frame readout. The latter property of the chip may be particularly useful for new detectors for the future **EIC (Electron-Ion Collider).**

## REFERENCES

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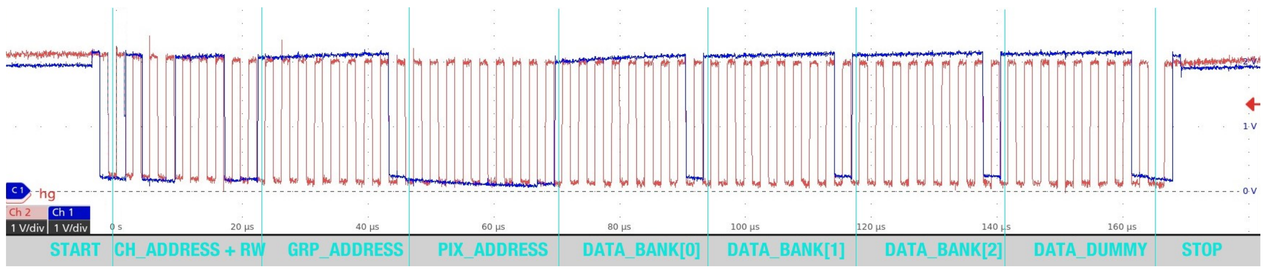


Fig. 6. An exemplary I2C command waveform used to change configuration

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