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An FPGA-based Front-end Module Emulator for the High Granularity Timing Detector

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Introduction

HGTD Functionality and Design

- The High Granularity Timing Detector[1](HGTD) is proposed as a part of the ATLAS Phase-II upgrade to mitigate the impact of pileup on object reconstruction by precisely measuring the time of tracks within the HGTD readout modules. The readout module is based on 2 ALTIROC[2] ASIC chips.
- The ALTIROC integrates 225 channels to readout 15×15 sensor cells of 1.3×1.3 mm². The ASIC provides a timing measurement as well as a luminosity measurement. The data of each of the 15 columns are read out by an end of column. The periphery integrates the digital blocks for the readout, the data serializer and the analog common blocks. The resulting data traverses a flexible PCB and the Peripheral Electronic Board (PEB) before being collected by the Data Acquisition system (DAQ). Simultaneously, the readout module handles the dual responsibilities of managing slow control information from the Detector Control System (DCS) and fast commands from the Time Trigger Control system (TTC).
- The HGTD readout module emerges as indispensable for testing both individual components and the full readout chain of the HGTD system.

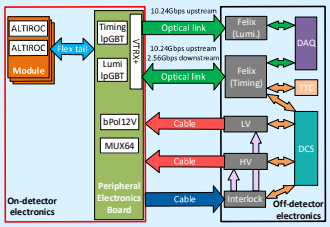

Figure 1. Schematic of the HGTD electronics system

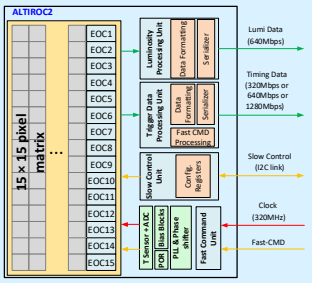

Figure 2. Logic schematic of ALTIROC

Challenges and Emulator Solution:

- Due to the protracted nature of ASIC chip design, the readout modules are inaccessible during the early stages of the project. In response, a front-end module emulator is developed based on the Xilinx-Spartan 7 FPGA (XC7S15-2CPGA196C). The emulator assumes a pivotal role in expediting system debugging processes and validating the digital logic design of the ALTIROC.

Design of the Emulator

Hardware Design

- The emulator meticulously adheres to the same physical dimensions, measuring 2×4 cm, and connector type (FH26W) as HGTD readout module. This design ensures that the emulator seamlessly conforms to the mechanical dimension prerequisites during installation.
- Central to the emulator's functionality is the integration of the Xilinx-Spartan XC7S15-2CPGA196C FPGA, which is programmed to emulate the readout module.
- A 16 MB NOR-FLASH memory is incorporated to securely store the configuration file, facilitating the emulator's operation.
- For debugging purposes, a high-frequency crystal oscillator capable of generating a clock signal up to 200 MHz is included.
- A dial switch is encompassed intended for hardware reset, ensuring effective reset control.
- An NTC sensor is integrated to enhance monitoring capabilities.

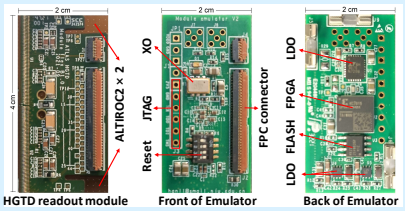

Figure 3. Dimensions of readout module and Emulator as well as the electronic components layout of Emulator

The amalgamation of these selected components forms the bedrock of the emulator's hardware design, poised to effectively replicate the functions of the readout module.

Firmware Design

The firmware translates the intricate digital functionalities of the readout module into four distinct logical functions, namely:

- Clock generator: The emulator harnesses the intellectual property (IP) resources of Xilinx to generate its requisite clocks based on a 40MHz external clock fed by the peripheral electronic board.
- Slow control unit: The logic code of this unit is directly transplanted from the ALTIROC design. The emulator's operational mode is determined by instantiating pivotal registers through I2C protocol.
- Fast command control unit: Responsible for receiving and deciphering fast commands dispatched by the TTC system, this unit is pivotal in acquiring trigger-related information for data acquisition.
- Data formatting and encoding: The FPGA is programmatically tailored to generate data for the 225 pixels, aligning with the readout module's data generation process. Upon receipt of a trigger, a data package is dispatched to a FIFO buffer. To maintain DC balance, the data undergoes encoding via an 8b10b encoder. The length of the data frame and the serialized output speed are adjustable according to configurations of the slow control registers.

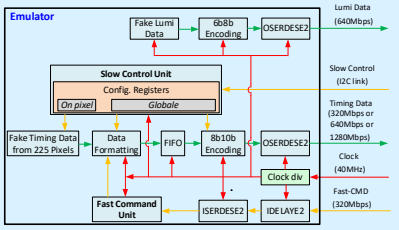

Figure 4. Logic schematic of Emulator

Application of the Emulator

The emulators establish connectivity with modular peripheral electronics board[3], a minimum demonstrator system with full-features of the HGTD to enable verifications of detector design. The emulator serves as a stand-in for the HGTD readout module in system debugging.

1. Sub-system debugging facilitated by the emulator: The emulator serves as a surrogate that aids in the comprehensive debugging of those sub-systems relying on HGTD readout module as transceiver.
   - Bit error rate test (BERT): To mitigate bit errors after a complex path transmission, configurable registers related to pre-emphasis are integrated into the detector design. Optimal values of these registers are determined based on eye-diagram scans performed with the emulator output as data source.

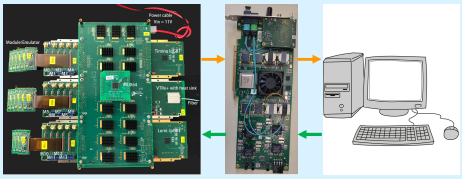

Figure 5. Minimum demonstrator system of HGTD

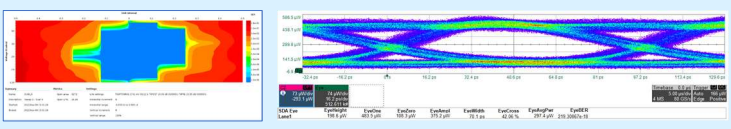

Figure 6. BERT test. (left) Eye-diagram tested with Xilinx IP. (right) eye-diagram tested with oscilloscope

- DAQ test: DAQ system is responsible for decoding and saving the received data package. This functionality is assessed using the emulator, whose data frame and encoding mode mirror that of the HGTD readout module.
- Fast command test: TTC system is responsible for sending fast commands to the readout module, providing trigger information for data acquisition. Within the emulator's framework, a dedicated fast command decoding unit is orchestrated to test and validate the functionality of the TTC system.

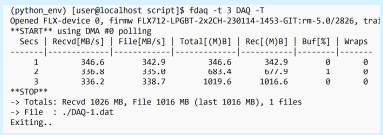

Figure 7. Data taking test

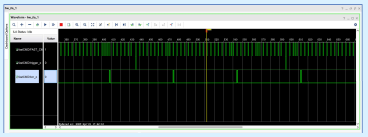

Figure 8. Fast command verification

- ADC calibration: The calibration of ADCs assumes prominence in monitoring the temperature and voltage of the HGTD. This crucial task is entrusted to the lpGBT ASIC, positioned on the PEB. Calibration of the ADC is effectively executed using the NTC sensor located on emulator.

2. Verification of chip design: The digital logic design for the slow control unit of ALTIROC is seamlessly transplanted to the emulator and verified to work as expected.

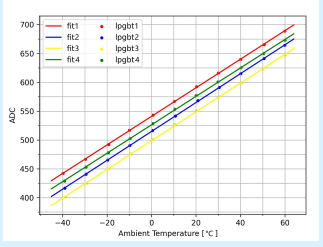

Figure 9. ADC calibration for 4 lpGBT chips

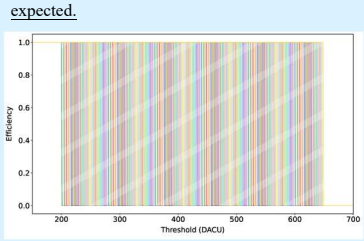

Figure 10. S-curve scanning of 225 pixels simulated using the Emulator

3. Full system debugging with emulator substitution: In full system tests, the emulator replicates the output characteristics of the readout module, encompassing data rate, encoding mode, and threshold discrimination across 225 pixels. The scripts developed for threshold scanning of various variables can also be applied to emulators for verification purposes.

Conclusion and outlook

We present an FPGA-based front-end module emulator tailored for the HGTD project in the ATLAS experiment. This emulator stands as a surrogate solution, effectively mimicking the functionality of the HGTD readout module during the project's initial design phase. Leveraging the capabilities of a Xilinx-Spartan 7 FPGA (XC7S15-2CPGA196C), the emulator adeptly replicates the intricate digital operations of the HGTD readout module to promote system tests and verifications. Moreover, the emulator offers an economical and versatile avenue to validate the digital logic design of ALTIROC before venturing into chip production.

The emulator's role extends beyond project-specific applications, highlighting its potential as a versatile tool for detector development and validation. This approach, as demonstrated by the HGTD project, could potentially find application in other experimental setups, fostering rapid progress and efficient validation in the realm of high-energy physics and beyond.

Reference

[1] ATLAS Collaboration, Technical Design Report: A High-Granularity Timing Detector for the ATLAS Phase-II Upgrade, ATLAS-TDR-031.
[2] R. C. Mohr et al., ALTIROC2, a readout ASIC for the High Granularity Timing Detector in ATLAS, presented at TWEPP 2019.
[3] L. Han et al. (ATLAS HGTD Group), Demonstration system of the HGTD peripheral electronics boards for ATLAS phase II upgrade, Nucl. Instrum. Methods Phys. Res. A, 1045 (2023), Article 167651.