Contribution ID: **36** Type: **Poster**

An FPGA-based Front-end Module Emulator for the High Granularity Timing Detector Readout Module

Thursday 5 October 2023 18:40 (20 minutes)

The HGTD aims to mitigate the effect of large pile-up interactions in the ATLAS Phase II upgrade project by providing accurate time measurements for tracks. However, since HGTD readout modules are unavailable during early stage, an FPGA-based front-end module emulator is designed as a substitute for system testing. This emulator also provides a flexible and cost-effective means to verify the digital logic of the ASIC chip used in the HGTD readout module. This presentation offers a solution for replacing ASIC chips with FPGAs during system test, and also provides a method for verifying the design of an ASIC chip.

Summary (500 words)

The large increase of pileup is one of the main experimental challenges for the High Luminosity LHC project (HL-LHC) physics program. A High-Granularity Timing Detector (HGTD) is proposed for the ATLAS Phase-II upgrade to measure the time of the tracks accurately in order to mitigate the effect of the pile-up in the object reconstruction. The time information of tracks is measured, encoded and formatted in the HGTD readout module based on the ALTIROC chip. The data are transmitted through a flexible PCB and the peripheral electronic board (PEB), and eventually are collected by the data acquisition system (DAQ). At the same time, the HGTD readout module is also responsible for handling the slow control information from detector control system (DCS) as well as the fast command from time trigger control system (TTC).

HGTD readout module is essential when testing the individual components as well as the full chain of the HGTD readout system. However, because of the lengthy ASIC chip design and manufacturing process, HGTD readout modules are unavailable in the early stage of the project. We design a front-end module emulator based on Xilinx-Spartan 7 FPGA (XC7S15-2CPGA196C) to mitigate the influence to HGTD tests. It realizes four primary functionalities of HGTD readout module.

Firstly, it generates pseudo time data of tracks, and then packages and encodes the data in the same manner as the HGTD readout module. The emulator plays a crucial role in bit error rate test for the HGTD DAQ path as data source. The test results in turn instruct us to determine the optimal parameters for pre-emphasis. Meanwhile, the emulator's output has the same encoding mode and data frame as HGTD readout module. As a result, it can be used to verify the decoding and storage functions of the DAQ.

Secondly, the emulator's fast command control unit receives and decodes fast commands from TTC, which helps verify different fast commands and their stability of transmission.

Thirdly, the slow control unit of the emulator ensures that we can configure the emulator to different working modes online.

Lastly, the emulator can generate analog signals which are feed to a dedicated mux chip on PEB, and then to the ADC of lpGBT chip located on PEB. These signals can be used to verify the mux chip and calibrate the ADC.

Besides the logic functions, the emulator shares same overall dimensions and connectors with HGTD readout module. These features allow that the emulator can substitute for HGTD readout module in system test while the HGTD readout module is unavailable.

In addition, the emulator also provides a cost-effective and flexible means to verify the design of the ASIC chip used in HGTD readout module. We transplanted the slow control simulation code of the ASIC chip to emulator and verified it works well.

The emulator has played a crucial role in HGTD project. It also offers a solution for replacing ASIC chips with FPGAs during system test, and also provides a method for verifying the design of an ASIC chip.

Authors: CASTILLO GARCIA, Lucia (IFAE - Barcelona (ES)); GE, Zhenwu (Nanjing University (CN))

Presenter: GE, Zhenwu (Nanjing University (CN))

Session Classification: Thursday posters session

Track Classification: Programmable Logic, Design and Verification Tools and Methods