An open-sorce IP-Core for Multi-Voltage Thresholding signal acquisition with FPGAs

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The Multi-Voltage Thresholding (MVT) approach [1], [2] offers an alternative to high-speed multichannel ADCs for signal acquisition. While the approach has similarities to comparator-based Flash-ADCs, it utilizes FPGA internal resources to replace external ADCs. This reduces costs, complexity, and energy consumption for applications that strongly require fast multichannel digitization, but are satisfied with a low ADC resolution.

One may note that most inputs in modern FPGAs are capable of operating in Low-Voltage Differential Signaling (LVDS) mode, which enables the implementation of MVT with LVDS differential receivers. LVDS receivers of an FPGA are not ideal and can have a positive or negative bias of up to $\pm 40mV$, which must be determined and compensated for every LVDS receiver through a calibration procedure. The calibration procedure involves applying a known voltage as a threshold and a test pulse of triangle form with exactly known parameters to the LVDS receiver. The bias of an LVDS receiver results in a switching delay (positive or negative) in respect to the predicted moment when the LVDS receiver should have switched. From the measured delay we calculate the needed bias compensation for the particular LVDS receiver.

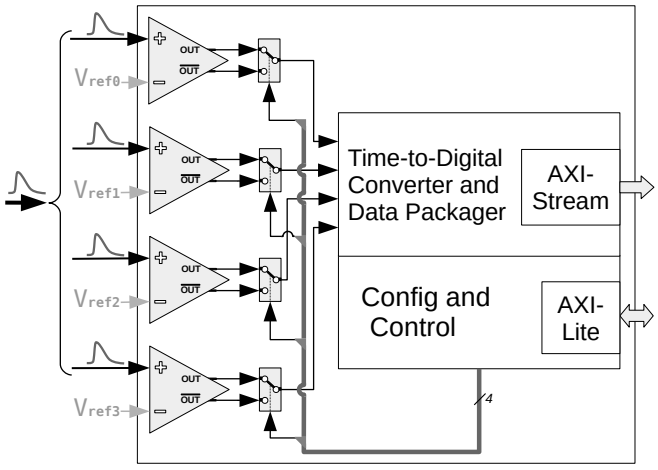

Figure 1: General structure of the MVT-Quad IP-Core

Our focus in this talk is on the introduction of an open-source IP-Core, which we have named MVT-Quad IP-Core. This IP-Core is designed to sample analog signal from a single input and is equipped with four LVDS receivers (see Fig 1). It enables users to easily and efficiently integrate the MVT approach into their FPGA designs. The IP-Core integrates a streaming output for the acquired data and a memory mapped interface for registers, which are relevant for calibration and configuration. To implement the MVT-based signal acquisition for multiple input channels in a particular FPGA design, one needs to instantiate the respective number of MVT-Quad IP-Cores and provide some minimal additional external schematics for the voltage thresholding. A reference design for this external schematics is also present in the scope of this talk.

The successful functioning of our IP-Core is demonstrated in a test application where signals from multiple SiPM sensors are acquired, allowing for the acquisition of cosmic muons with scintillating stripes (see Fig. 2). This contribution provides an overview of the calibration procedure and how the LVDS receiver's bias may depend on parameters like the applied threshold voltage and temperature of the FPGA chip. Some further technical aspects, and possible difficulties and ways to overcome them are considered as well. Overall the MVT approach,

Figure 2: A test mezzanine board, implementing schematics for eight MVT signal-acquisition channels.

together with the proposed MVT-Quad IP-Core, has the potential as a viable solution for fast multichannel signal acquisition in various applications.

References

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