An open-sorce IP-Core for Multi-Voltage Thresholding signal acquisition with FPGAs

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Motivation and Introduction

High-speed multichannel ADCs are costly and require complex FPGA firmware to communicate with. The Multi-Voltage Thresholding (MVT) approach [1] offers an alternative to a high-speed multichannel ADC by harnessing the internal resources of an FPGA, reducing complexity and costs. We introduce an open-source IP-Core that simplifies use of the MVT method with a conventional FPGA. We also provide an overview of characterization measurements and specific calibration methods. Our example application demonstrates usage of the IP-Core for signal acquisition from multiple Silicon Photo-Multipliers (SiPMs) with the sampling rate of 800 MSPS.

MVT Concept basics

The Multi-Voltage Thresholding (MVT) follows the same principles as Flash-ADCs. It involves a voltage ladder for reference, comparators for input comparison, and a digital encoding circuit.

A significant advantage of this approach is its rapid digitization capability. However, it has a drawback: achieving higher resolution requires a substantial number of comparators.

Modern FPGAs feature differential receivers for Low-Voltage Differential Signaling (LVDS) inputs which in their core contain comparators. These comparators can be utilized for MVT [1,2]. The voltage references can be generated by slow and inexpensive multi-channel DACs.

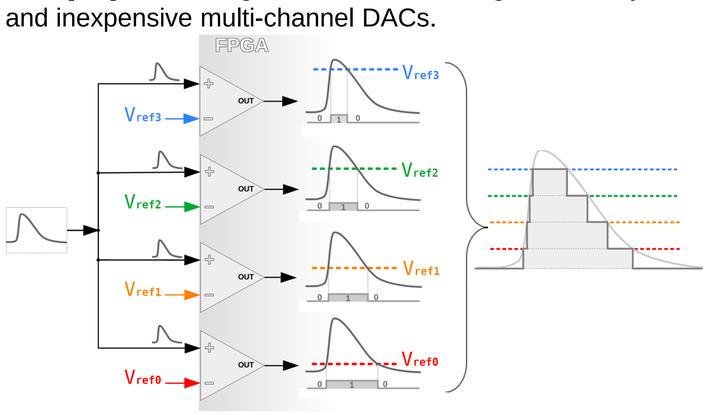

Fig. 1: Implementing the MVT concept within an FPGA.

Depending on the reference voltage level, the comparators have different transition- and on-times, which are registered by the proposed IP-Core.

FPGA intrinsic biases and calibration procedure

The intrinsic bias of FPGA input comparators can reach up to ±35mV [3]. It is important that the reference voltages provided for the comparators compensate the individual bias voltage of the respective comparator. A simple method for measuring the bias of a particular comparator is applying a triangle pulse with exactly know characteristics (length and amplitude).

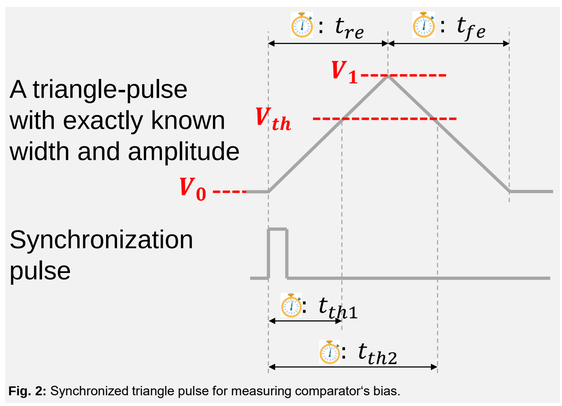

Fig. 2: Synchronized triangle pulse for measuring comparator's bias.

Δt_{th1} and Δt_{th2} are time-shifts with respect to the times when an ideal comparator would have switched on rising- and falling edges respectively. From the time-shifts the bias voltages ΔV_{re} and ΔV_{fe} are calculated. Repeating this procedure many times and plotting each calculated point results in a comparator's characteristic distribution (see Fig. 3).

$$\Delta V_{re} = \frac{(V_1 - V_0)\,\Delta t_{th1}}{t_{re}}$$

ΔV_{re} bias values calculated from rising edge of triangle pulse

$$\Delta V_{fe} = \frac{(V_1 - V_0)\,\Delta t_{th2}}{t_{fe}}$$

ΔV_{fe} bias values calculated from falling edge of tirangle pulse

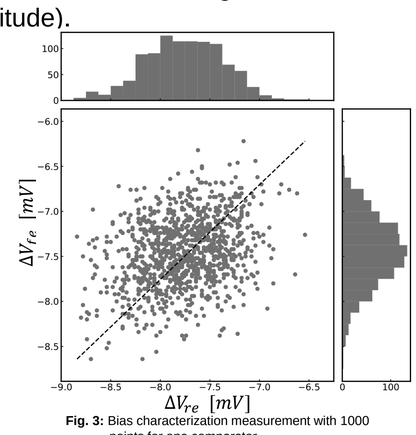

Fig. 3: Bias characterization measurement with 1000 points for one comparator.

When the bias measurement procedure is performed on four comparators, it results in a plot featuring four distinct distribution clusters.

Each cluster corresponds to the bias of a specific comparator. The determined bias voltages are to be compensated by applying pedestal values to the DAC-channels, providing reference voltages at the respective comparators.

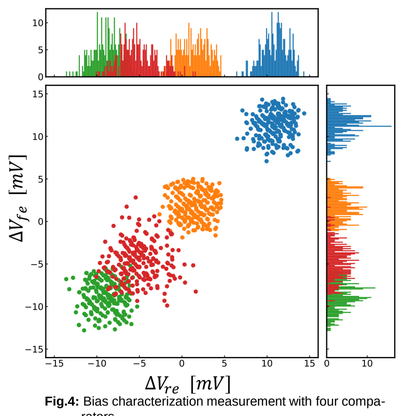

Fig.4: Bias characterization measurement with four comparators.

Calibration procedure
After applying the compensation pedestal voltages for every comparator's reference, repeating the calibration procedure results in near-zero bias shift for all four channels.

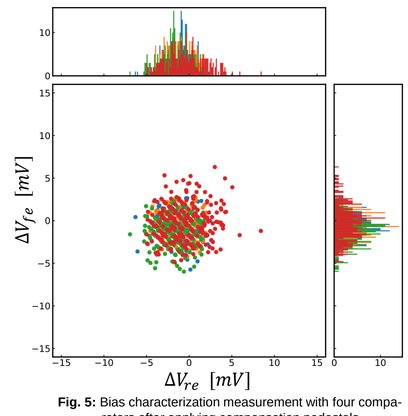

Fig. 5: Bias characterization measurement with four comparators after applying compensation pedestals.

MVT Quad IP-Core

The IP-Core is equipped with four sampling inputs and therefore is referred to as an MVT-Quad. Each input comparator is followed by a deserializer responsible for Time-to-Digital Conversion (TDC).

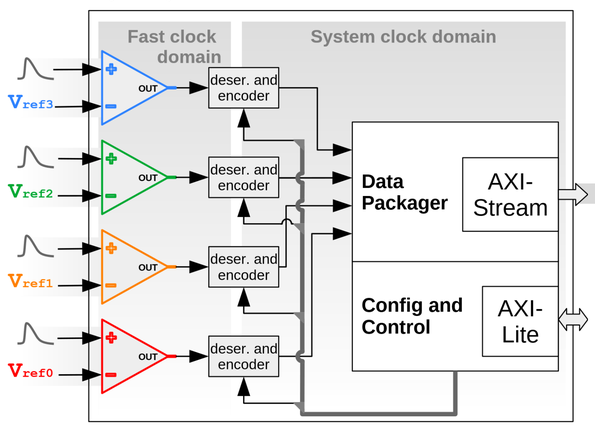

Fig. 6: MVT Quad IP-Core structure.

Deserializers operate in a fast clock domain (in our example application 800 MHz) and therefore capturing the signal transitions with high time-resolution. Resulting TDC values come to the Data-Packager.

The IP-Core features two interfaces: AXI-Stream and AXI-Lite. The AXI-Stream interface streams out the TDC values of signal transitions. AXI-Lite interface is dedicated for interfacing internal configuration registers.

The MVT-Quad IP-Core is an open-source project distributed under CC BY-SA 4.0 license. The project is evolving at http://git.rwth-aachen.de/muon-hodoscope/mvt_quad_ip

Output data format

AXI-Stream data transmission is initiated whenever one or more comparators switch. Having at least one valid TDC-value from one comparator, the Data-Packager prepares a 32-bit wide word which is streamed out via AXI-Stream master interface. This 32-bit word can contain the information on up to two transitions (rising- and falling- edges) which took place within one period of the system clock for every of the four comparators. The AXI-Stream data transmission starts with a 32-bit word which carries the value of the system-clock counter register, serving as a raw time-reference. All the subsequent 32-bit payload words contain addendums from the high-speed clock domain.

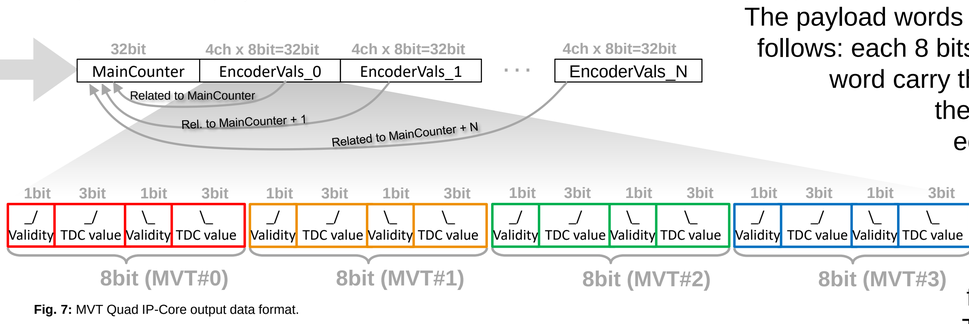

Fig. 7: MVT Quad IP-Core output data format.

The payload words are structured as follows: each 8 bits within the 32-bit word carry the information on the rising and falling edge transitions of one comparator. If any transition took place, the validity bit for the respective TDC-value will be set to "1". If no transitions are registered on any of the MVT Quad comparators within one period of the system clock, the AXI-Stream transmission is ended

FPGA resources utilization

The below tables give an overview of the resources utilization of an FPGA for instantiating one MVT Quad IP-Core.

1. CLB Logic

Site Type	Used
CLB LUTs*	213
LUT as Logic	213
LUT as Memory	0
CLB Registers	397
Register as Flip Flop	397
Register as Latch	0
CARRY8	12
F7 Muxes	0
F8 Muxes	0
F9 Muxes	0

4. I/O

Site Type	Used
Bonded IOB	8

5. CLOCK

Site Type	Used
GLOBAL CLOCK BUFFERs	1
BUFGCE	0
BUFGCE_DIV	1
BUFG_PS	0
BUFGCTRL*	0
PLL	0
MMCM	0

Naturally, the IP-Core fully utilizes the I/O infrastructure of four differential inputs. With it, the usage of resources on data packaging tasks and organizing interfaces is quite modest. It's however important to note that as the IP-Core evolves continuously, the extent of resource utilization may undergo changes.

8. Primitives

Ref Name	Used	Functional Category
FDRE	392	Register
LUT2	103	CLB
LUT6	76	CLB
LUT3	41	CLB
LUT4	37	CLB
LUT5	20	CLB
CARRY8	12	CLB
FDSE	5	Register
LUT1	4	CLB
ISERDESE3	4	I/O
IBUFCTRL	4	Others
DIFFINBUF	4	I/O
BUFGCE_DIV	1	Clock

Example application

The MVT Quad IP Core was tested with help of a specifically developed FPGA Mezzanine Card (FMC). It provides the electronic base for eight analog inputs. Each analog input is equipped with a 4-channel 10-bit DAC (LTC2635), providing four reference voltages for the respective MVT Quad IP-Core. DAC values are loaded via the common I2C bus as shown in Fig. 8. The developed MVT FMC module is a part of a test-setup (see Fig. 9).

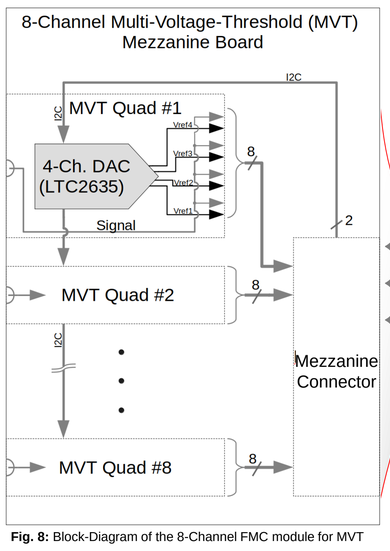

Fig. 8: Block-Diagram of the 8-Channel FMC module for MVT

Along with the MVT FMC module, the test-setup includes the TE0820 System-on-Module (SoM) having the Zynq Ultrascale+ chip in its core and the carrier module TE0701. Both SoM and carrier module are from Trenz Electronic GmbH [4].

The setup was tested with the sampling rate of 800 MSPS for acquiring output pulses from SiPM-based frontends, used in a stripe-hodoscope shown in Fig. 10.

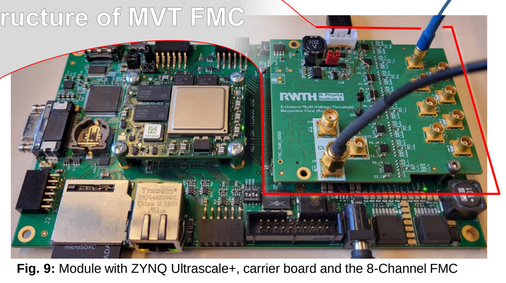

Fig. 9: Module with ZYNQ Ultrascale+, carrier board and the 8-Channel FMC

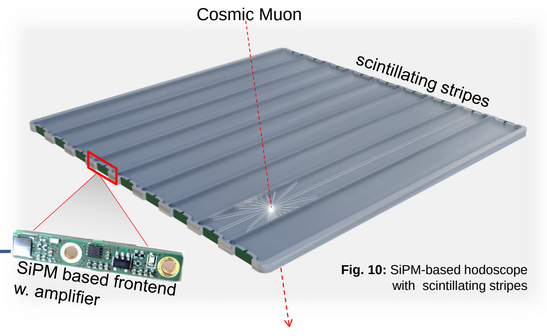

Fig. 10: SiPM-based hodoscope with scintillating stripes

The stripe-hodoscope is able to detect cosmic muons with a spatial resolution of ~2.5 cm. The scintillation light is detected by MicroFJ-30035 SiPMs, housed within a front-end circuit.

References

[1] Xi, Daoming, et al. "FPGA-Only MVT digitizer for TOF PET." IEEE Transactions on Nuclear Science 60.5 (2013): 3253-3261
[2] Moskal, Paweł, et al. "A novel method based solely on field programmable gate array (FPGA) units enabling measurement of time and charge of analog signals in positron emission tomography (PET)." Bio-Algorithms and Med-Systems 10.1 (2014): 41-45
[3] UltraScale Architecture SelectIO Resources, Datasheet UG571 v1.14. (2022): 33
[4] Website Trenz Electronic GmbH: https://www.trenz-electronic.de/en/

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