An open-sorce IP-Core for Multi-Voltage Thresholding signal acquisition with FPGAs

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Basic principle of Multi-Voltage Thresholding (MVT)

The basic principle of the presented concept is the same as with Flash-ADCs:

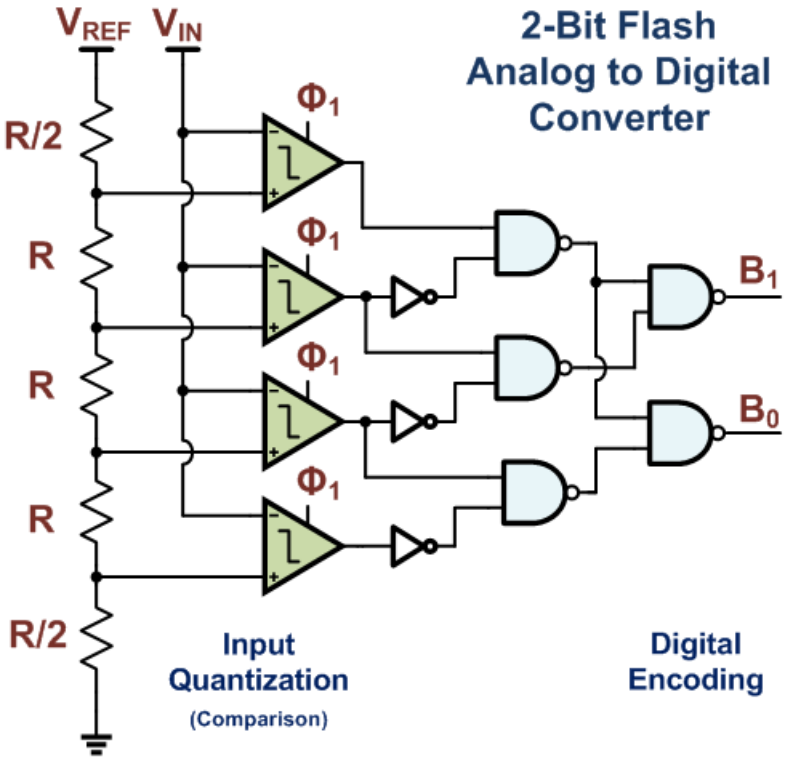
- **Voltage ladder** (providing ref. Voltages),
- **Comparators** (compare the input voltage to successive reference voltages),
- **Digital encoding circuit** (digital output)

Pro:

- Concept enables very fast digitization

Drawback:

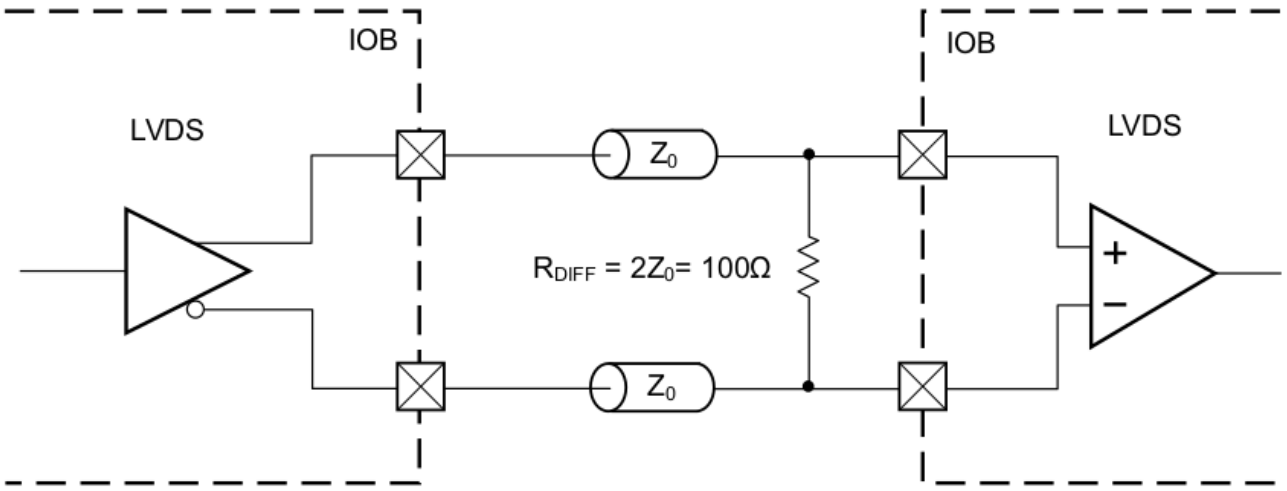
- Higher resolution demands a huge number of comparators $(2^n - 1)$



2-bit flash-ADC with digital encoding circuit (source: Wikipedia)

FPGA-intern comparators

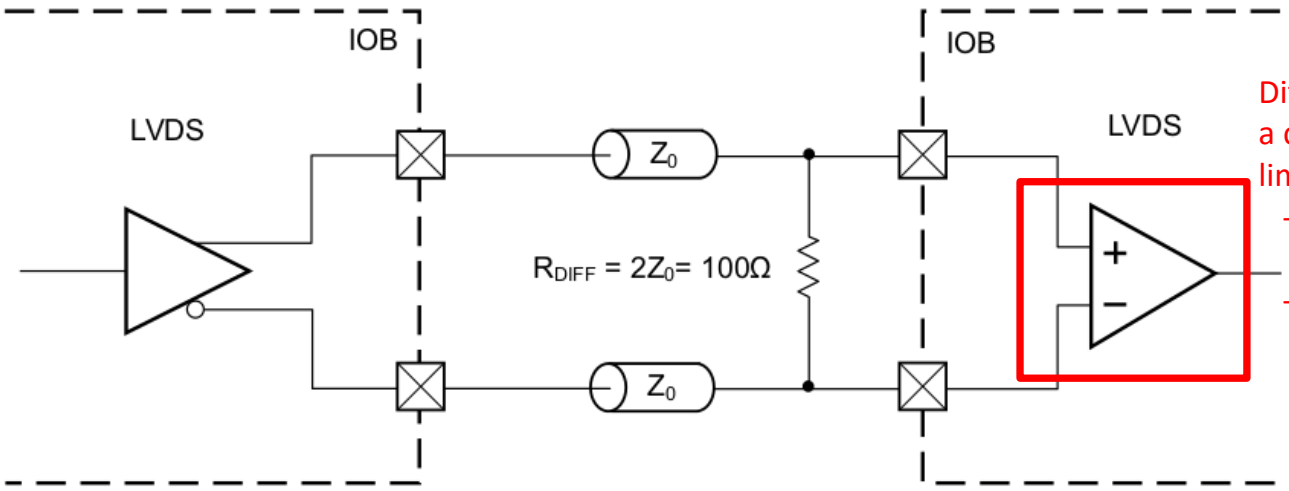
Most of the FPGA pin pairs are capable of Low-Voltage Differential Signaling (LVDS)



Input-Output Block. Source: Xilinx Datasheet UG571.

FPGA-intern comparators

Typically most FPGA pins can work in differential mode.
Let‘s use FPGA‘s diferential receivers for implementing a flash-ADC

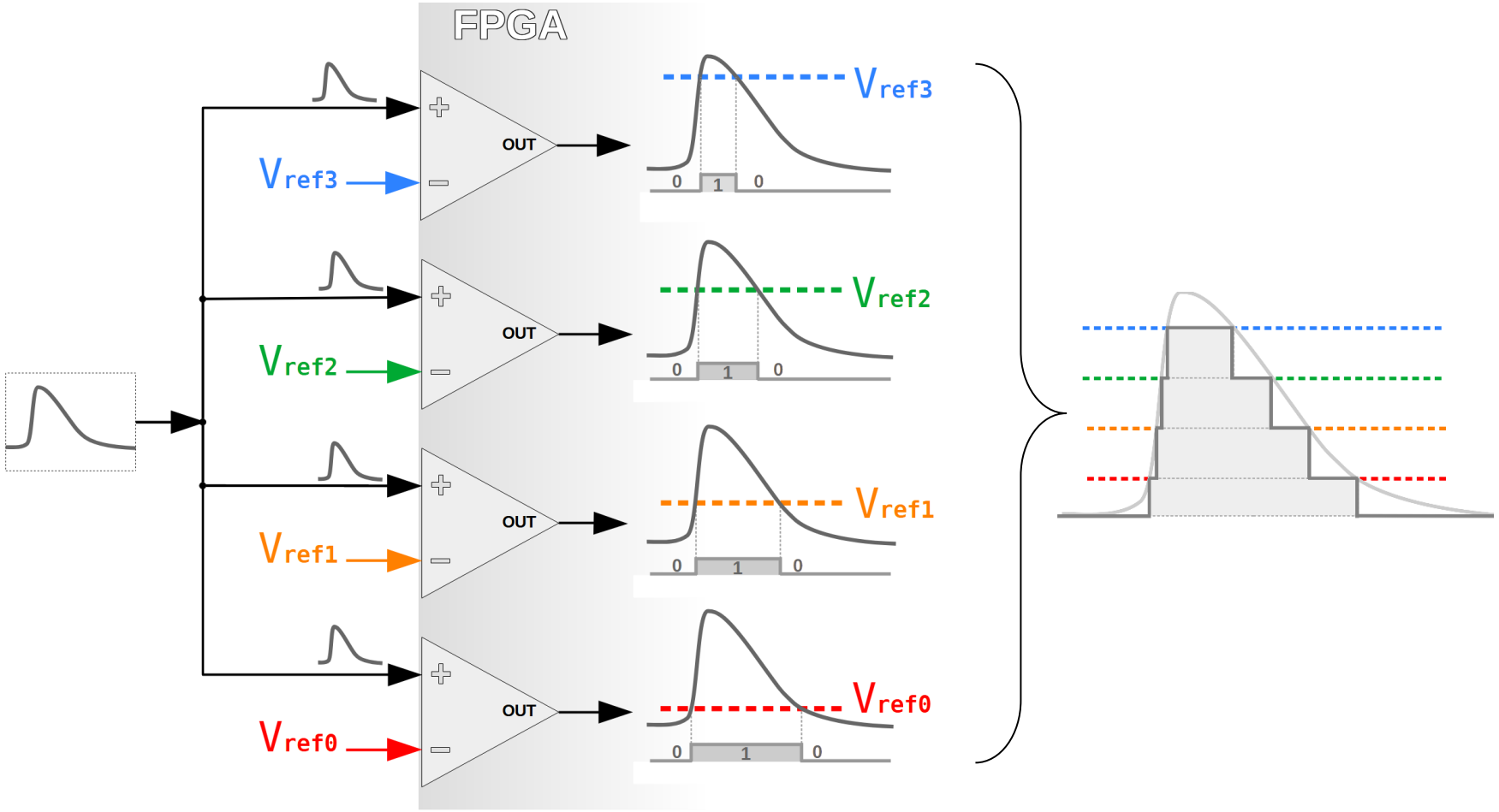


Differential receiver is a comparator with some limitations:
- Common voltage offset: 0,6 V to 1,1 V
- Max. differential amplitude: 600 mV

Source: Xilinx Datasheet UG571. Abbreviation IOB stands for Input-Output Block

MVT-Quad IP-Core

Our IP-Core enables implementation of four LVDS-comparators. Sampling rate tested: 800MSPS



An eight-channel FMC-module and an implementation example are present in the poster as well