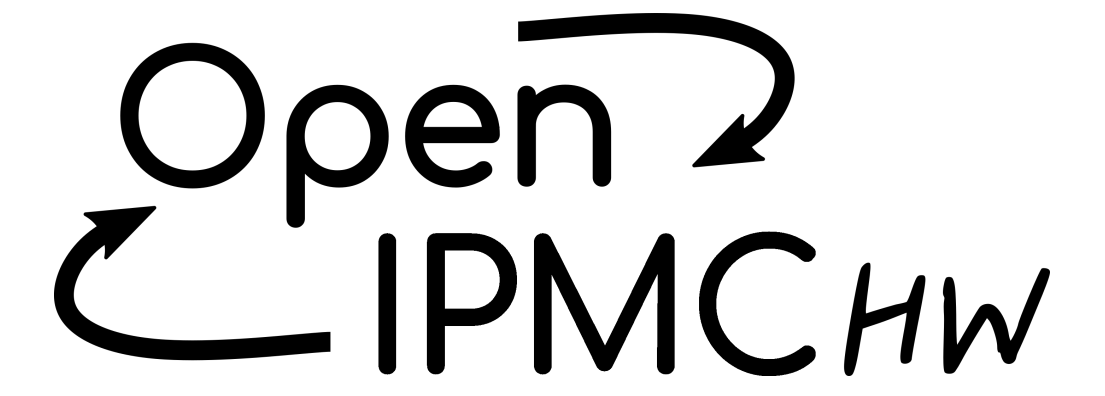


Novel developments on the OpenIPMC project



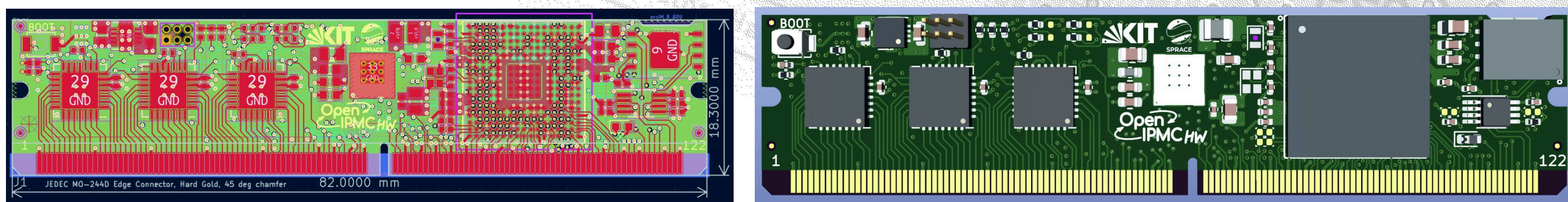
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Introduction and context

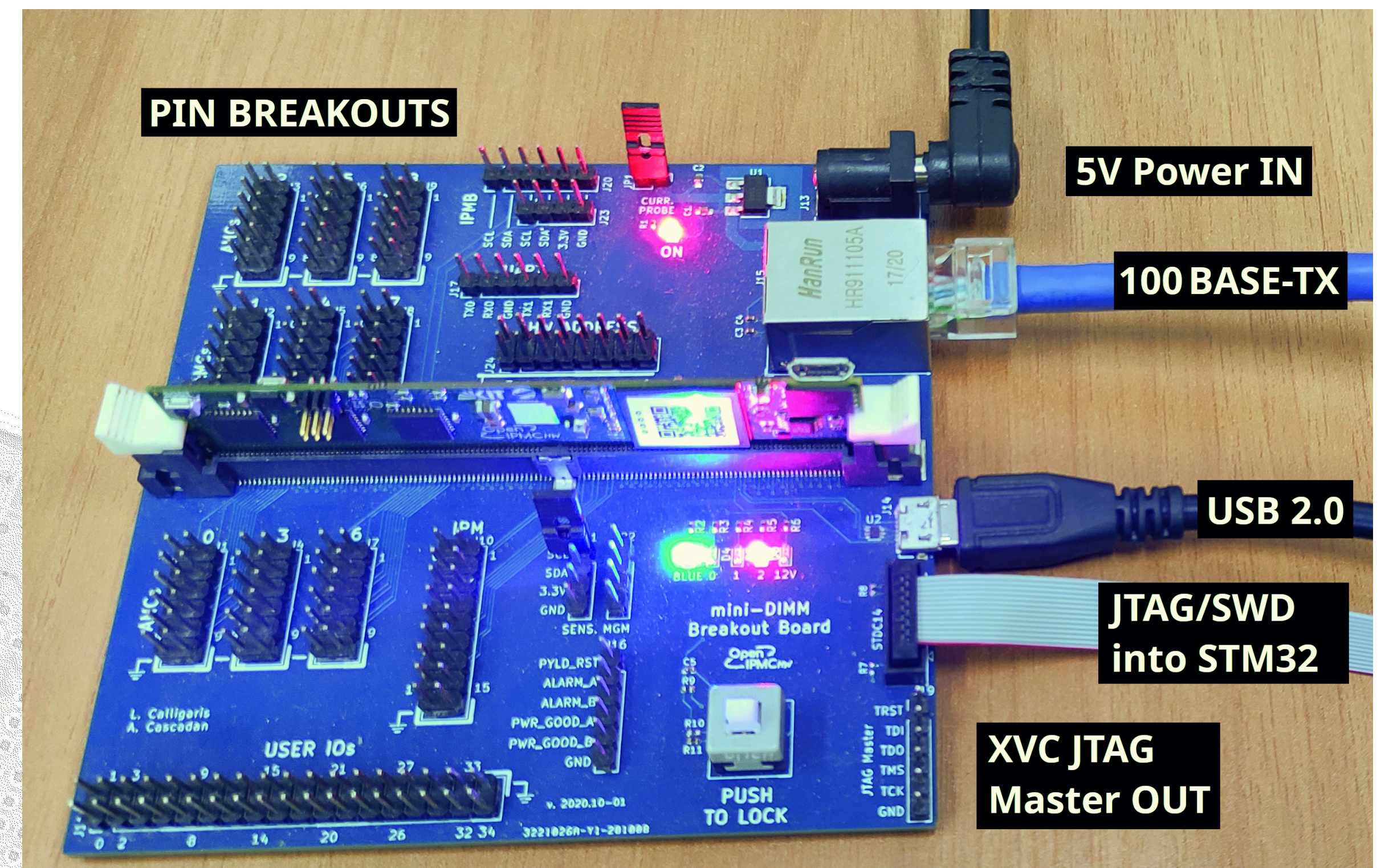
Numerous high-performance read-out, trigger and DAQ boards designed for upgrades of HL-LHC experiments, such as Pulsar-2b, Apollo and Serenity, comply with the ATCA standard, requiring them to use an Intelligent Platform Management Controller.

The OpenIPMC project aims to develop a free, open-source and fully customizable IPMC based on moderate-cost components.



The project consists of a platform-independent software (OpenIPMC-SW) implementing the IPMI behavior, a firmware (OpenIPMC-FW) merging IPMI with additional functions and an IPMC mezzanine (OpenIPMC-HW) tailored for the application. This mezzanine is pin-compatible with the ATCA boards named above.

The mezzanine is based on a powerful STM32H745/755 MCU. The software toolchain is free, based on GCC, GDB, FreeRTOS and Eclipse.



OpenIPMC-HW in its development breakout board

YAFFS storage, config DB, TFTP

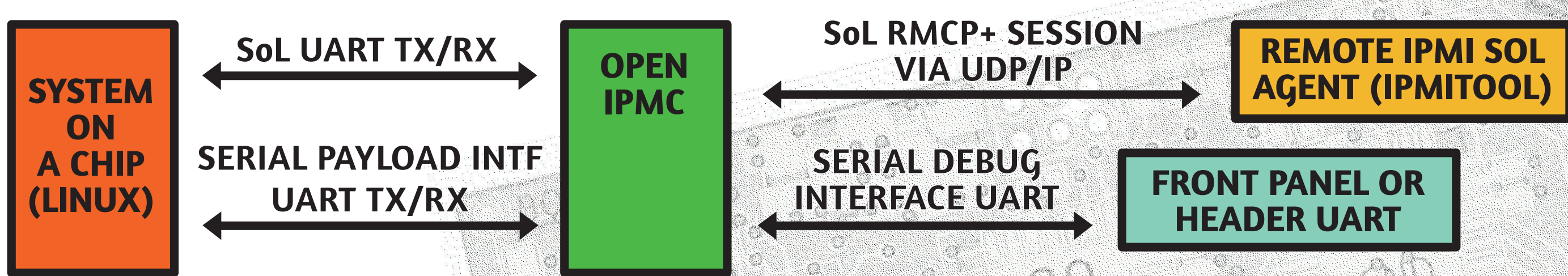
The Yet Another Flash File System (YAFFS2) was integrated in the firmware, allowing to mount regions of the external 1Gbit NAND flash as a file system, and manipulate its files via CLI terminal.

Firmware configuration parameters, such as DHCP configuration, are stored as text files in the file system, making them easy to change by the end user.

A TFTP server is included in the firmware, exposing the content of the file system to the IP network and allowing batch programming a large set of boards via a central network controller.

```
>> ls
etc          inode 257      length 2032    drw- directory
lost+found  inode 2       length 2032    drw- directory
>> ls etc/
syslog.conf  inode 513     length 21      -rw- data file
>> print /etc/syslog.conf
~ syslog.ip=10.0.0.172
~
print: 21 bytes read
>> |
```

SoL, Payload and Debug Interfaces



In the expected target boards the IPMC will co-exist with a SoC running Linux. This SoC will communicate with the IPMC over:

- Serial over LAN (SoL) interface, which will pipe the SoC boot and Linux terminals over an RMCP+ session via UDP/IP for Linux debug and recovery purposes.
- Serial Payload Interface UART, allowing reciprocal control between SoC and IPMC, e.g. to reboot Linux or get the Shelf ID.

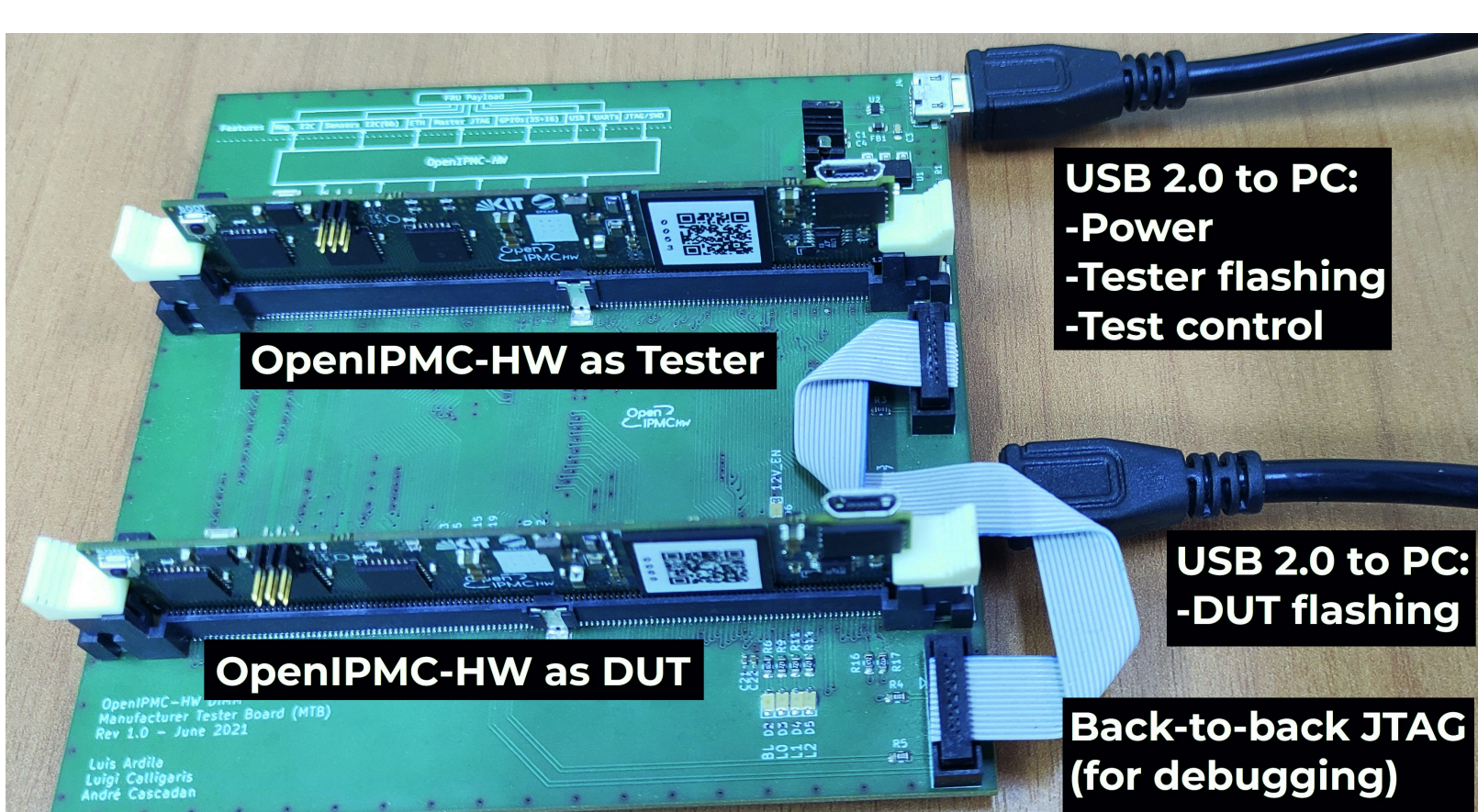
Additionally, a Serial Debug Interface UART is exposed to the carrier board for connection on a header or on the front panel. This interface provides access to the IPMC CLI. This CLI is also accessible on a virtual console over USB and over telnet.

Hardware v 1.2, manufacturing

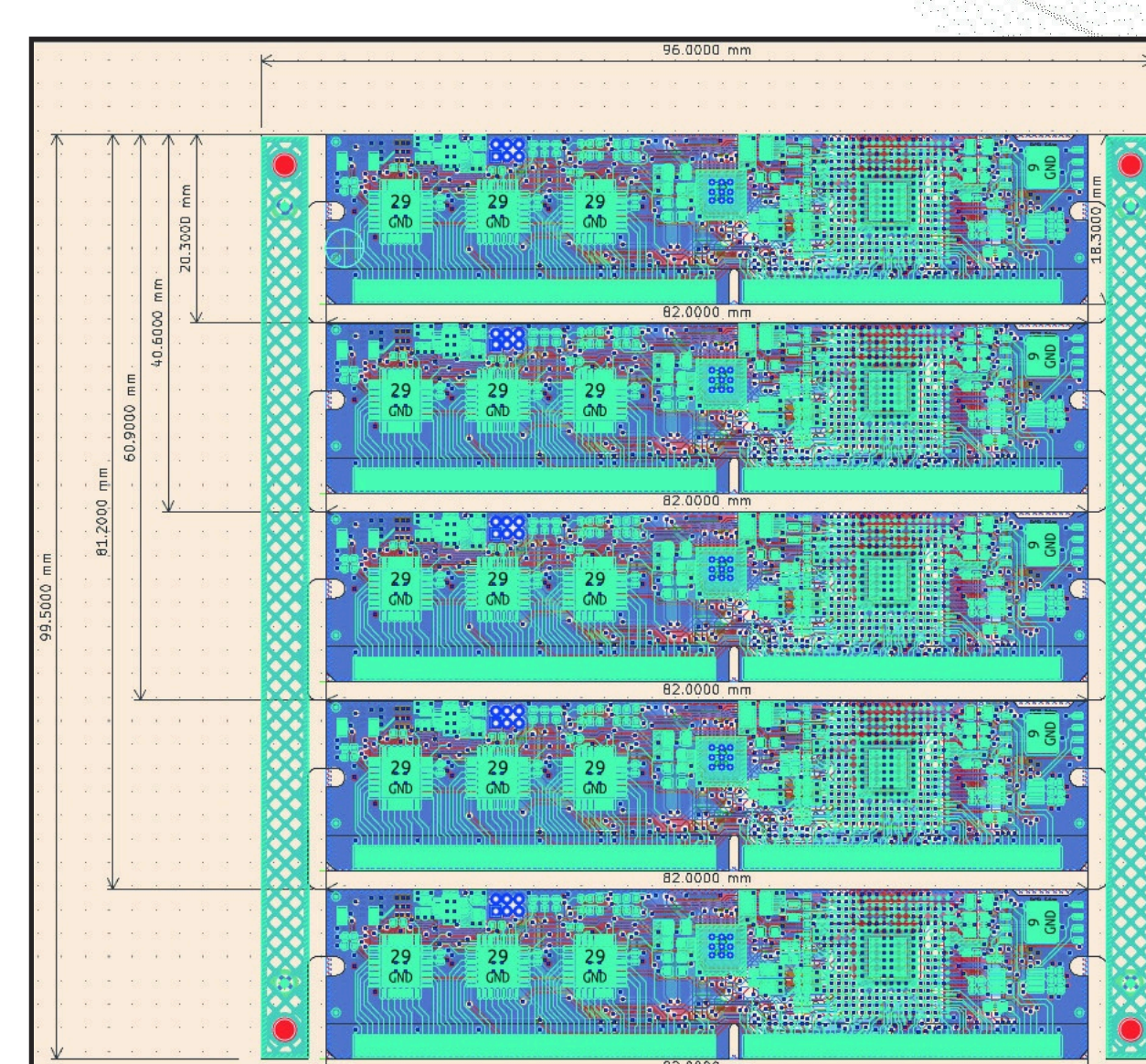
A new version (v1.2) of OpenIPMC-HW will provide a number of improvements resulting from the extensive tests of the past 2 years.

The changes introduce the capability of the "payload power enable" signal to hold its state upon an IPMC cold reset, as recommended by the ATCA standard (PICMG 3.0 R3.0 REQ 3.185), along with a number of minor improvements.

Iteration with companies involved in the production of the PCBs and their assembly is ongoing, to optimize the design to the relevant IPC manufacturing standards.



OpenIPMC-HW post-manufacturing test board



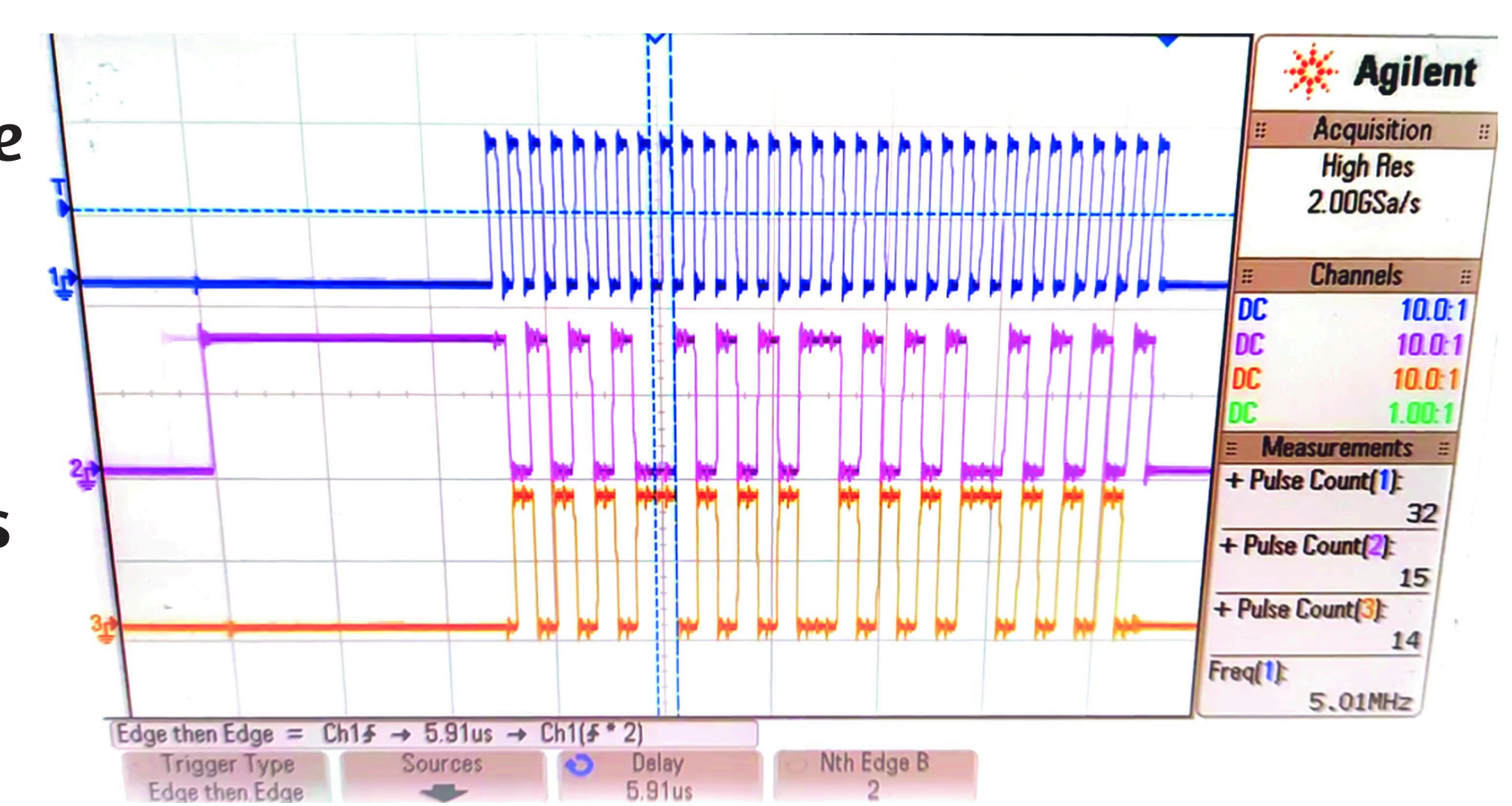
PCB panel design for production

Xilinx Virtual Cable server

Support for the Xilinx Virtual Cable protocol was added, allowing to operate a bit-banged JTAG master interface through a network connection to program and debug Xilinx FPGAs.

The JTAG interface is implemented via hardware offloading, reducing the use of CPU resources.

The XVC server has been tested on 6-series, 7-series and Ultrascale+ Xilinx devices, reaching a top measured JTAG burst speed of 5 MHz.



JTAG Interface producing a test pattern at 5 MHz

Syslog support

Monitoring the large number of IPMC devices in the future LHC experiments can be accomplished with a Syslog collector. We added support for the Syslog protocol in the firmware, and tested its interoperability with Grafana Loki. The user can choose to use either the RFC 3164 or the newer RFC 5424 specification for the protocol.

Links and contacts

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