TWEPP 2023

Topical Workshop on Electronics for Particle Physics

GEREMEAS (CA) – 2023/10/06

Front-End Board for Large Area SiPM Detector

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on behalf of the JUNO collaboration

ROMA TRE UNIVERSITÀ DEGLI STUDI

JUNO

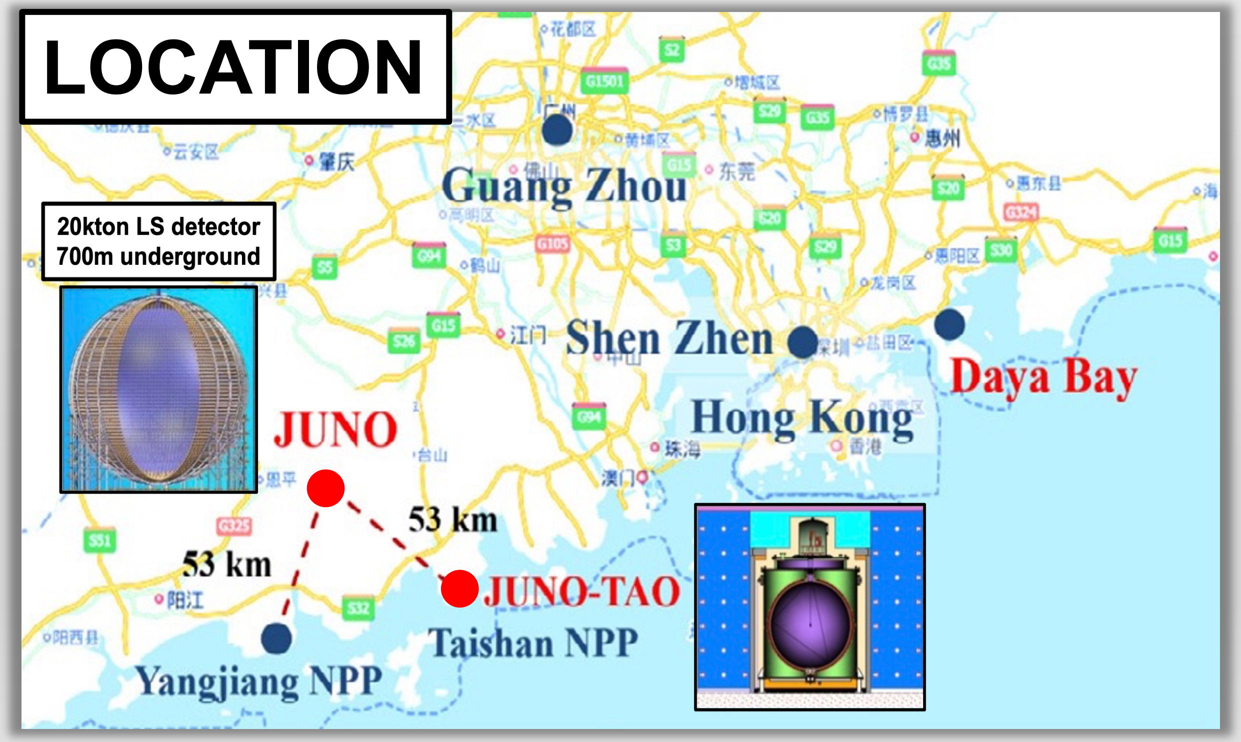
INFN

Outline

- JUNO-TAO Experiment
- Silicon Photo-Multipliers
- Read-Out Electronics
- Experimental setup & instruments
- Figures of merit & characterization
- Conclusions

JUNO-TAO Experiment

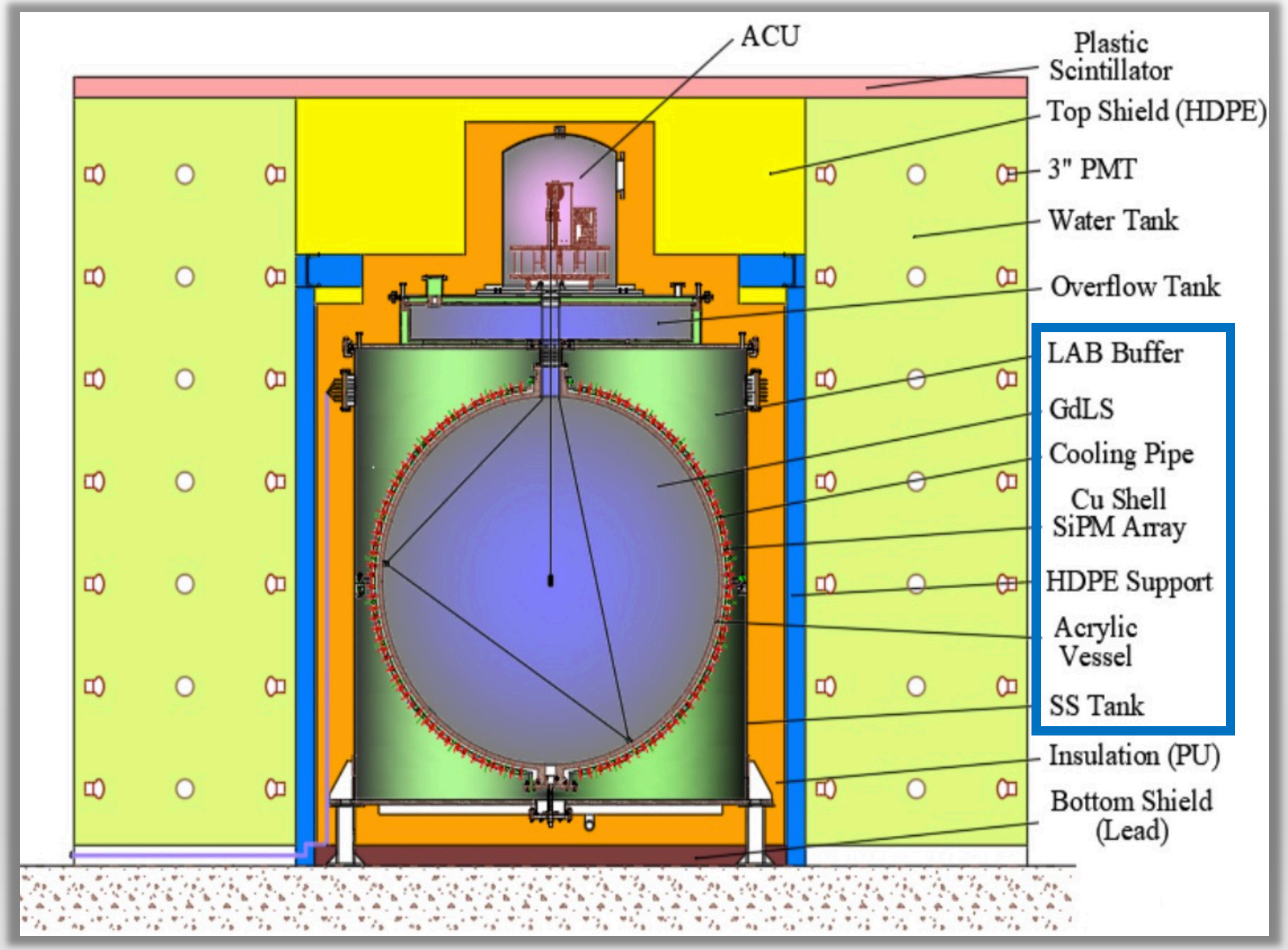
- The **T**aishan **A**ntineutrino **O**bservatory (**TAO**) is a satellite experiment of the **J**iangmen **U**nderground **N**eutrino **O**bservatory (**JUNO**), located in the southern China, expected to start collecting data in 2024.
- TAO consists of a spherical ton-level **G**adolinium-**d**oped **L**iquid **S**cintillator (**Gd-LS**) detector (1.8 m diameter) at ~30 m from a reactor core of the Taishan Nuclear Power Plant (4.6 GW) in Guangdong.
- By means of 10 m^2 SiPM covering the spherical LS, the reactor antineutrino spectrum will be measured with a sub-percent energy resolution (≤ 2% / √E MeV).



MOTIVATION

- ✓ Provide a model-independent reference spectrum for the JUNO neutrino mass-hierarchy measurement.
- ✓ Provide a new benchmark measurement to test nuclear databases.
- ✓ Reactor monitoring: status/fuel.

JUNO-TAO Central Detector



CENTRAL DETECTOR (CD)

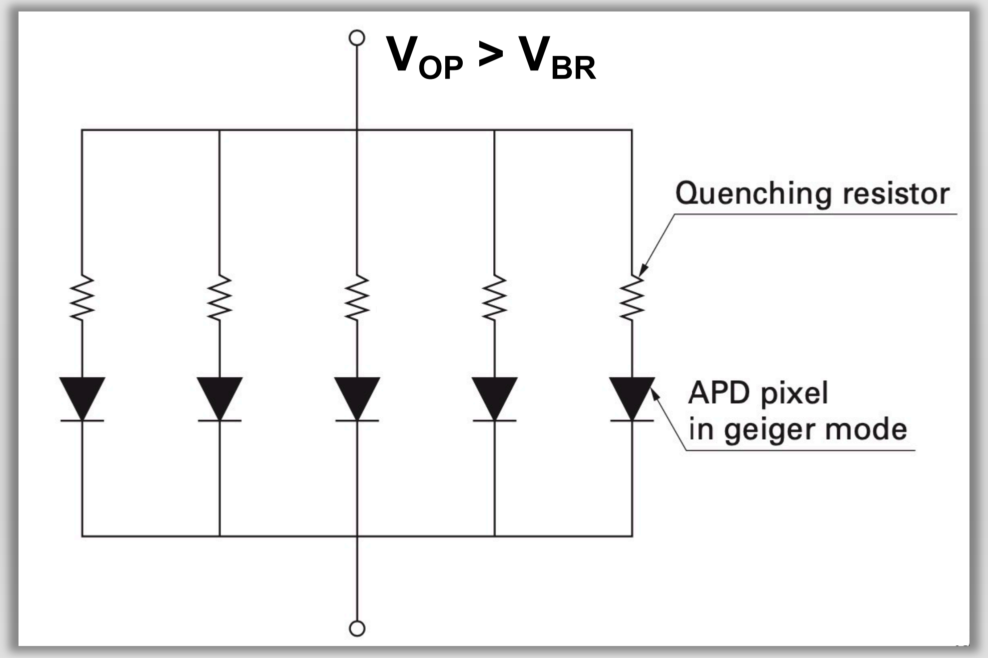
- Acrylic Sphere (d=1.8m, 20mm-thick) filled with 2.8t Gd-LS
- Copper Shell (d=1.886m, 12mm-thick) with SiPM tiles support
- SS Tank (d=2.09m, 10mm-thick) filled with 3.2t LAB/Gd-LAB
- Cryogenic System, at -50°C to reduce thermal noise
- Front-End Electronics (FEE)

❖ **The central detector operates at -50°C, inside a cryostat, to lower the dark/thermal noise of the SiPMs.**

Silicon Photo-Multipliers

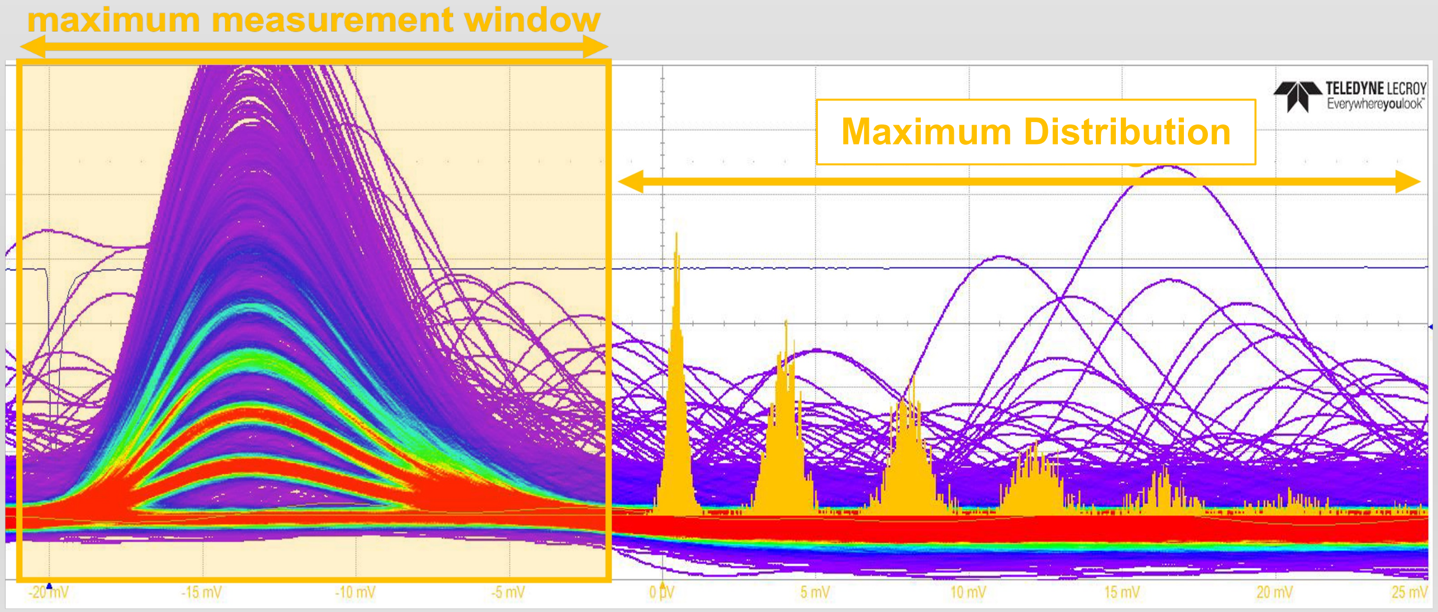
- **Si**licon **P**hoto-**M**ultipliers (**SiPMs**) are single-photon-sensitive devices based on arrays of many small **S**ingle **P**hoton **A**valanche **D**iodes (**SPADs**) connected in parallel.
- Each SPAD works in Geiger mode, and it is integrated with its passive quenching resistor.
- The output charge of the SiPM is the sum of all the charges generated by the fired SPADs, and it is proportional to the number of detected photons (**M**ulti-**P**ixel **P**hoton **C**ounter, **MPPC**)

SiPM Simplified scheme



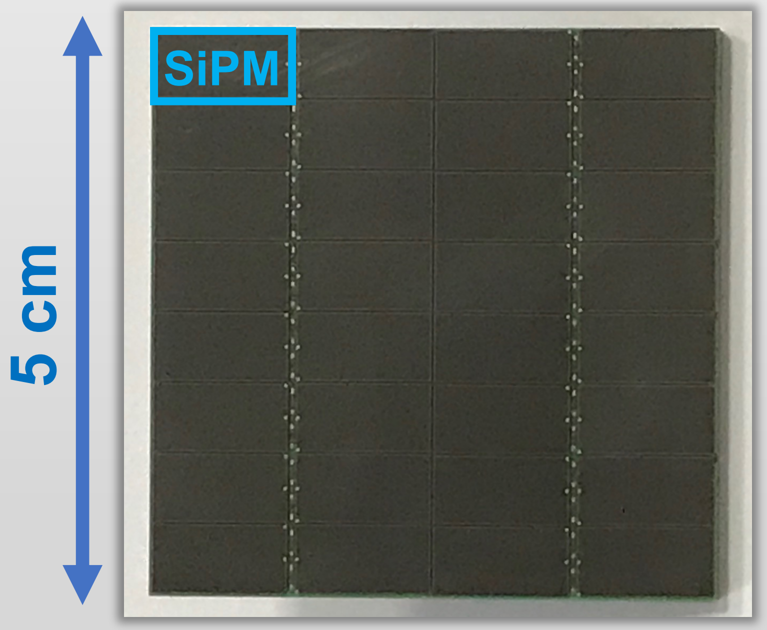
Typical acquired waveforms from the tile @ -50°C

Histogram related to the maximum of each acquisition in a defined time window



Hamamatsu SiPM Tile

- The total area of the TAO sphere is ~10 m^2, resulting in ~1.3 x 10^5 SiPMs. For installation and readout considerations, the SiPMs are assembled in ~4000 SiPM tiles of 8x4 SiPMs, with dimensions ~50x50 mm^2.
- In order to reduce the number of channels, multiple SiPMs are combined in one readout channel, with serial/parallel connection.



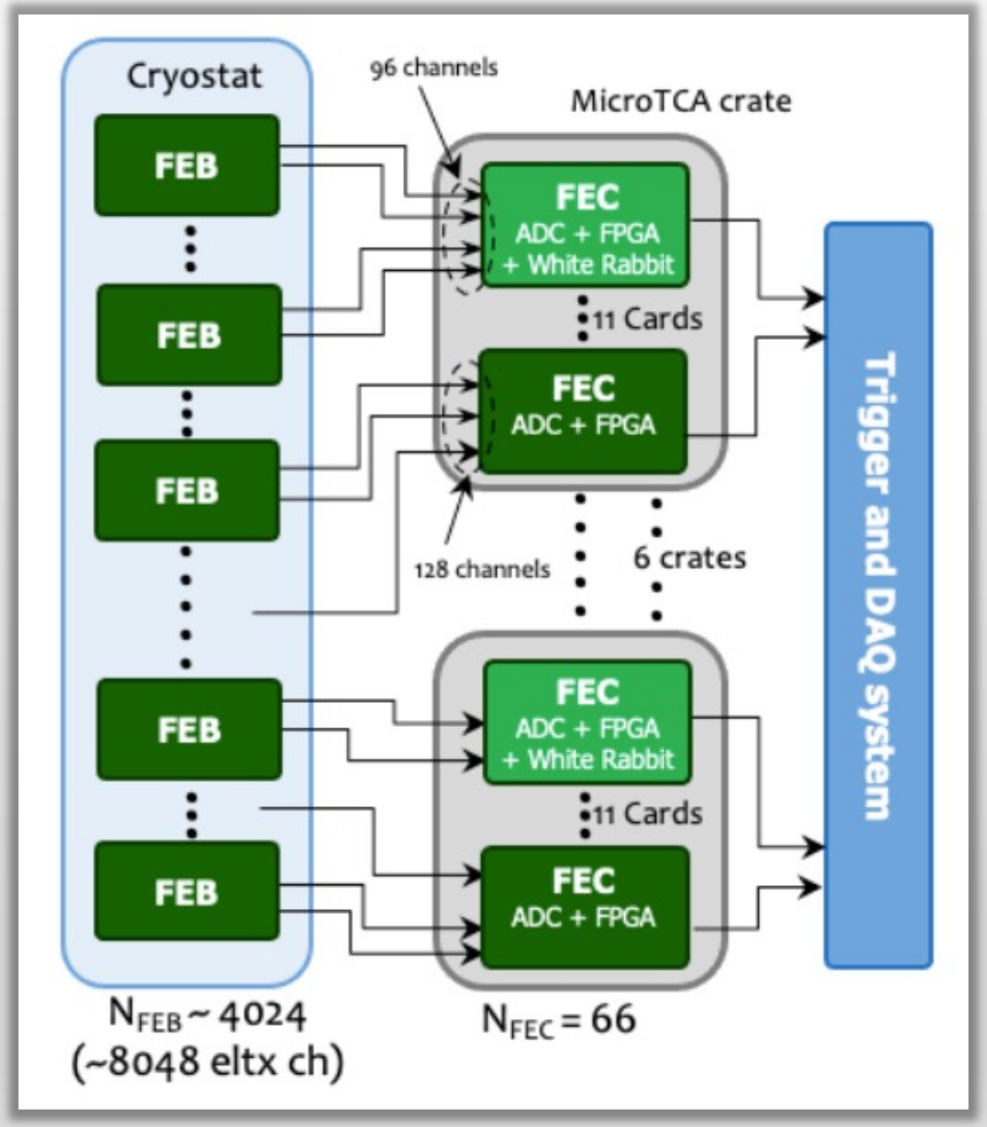
HAMAMATSU

S16088: SiPM TILE

- 12,782 SPADs x SiPM (75 μm pixel pitch)
- 8x4 array of 12x6 mm^2 SiPMs (5x5 cm^2)
- 10 m^2 / 25 cm^2 ≈ 4000 SiPM tiles
- Each SiPM tile splitted in 2 readout channels (with series/parallel connections)
- Each tile delivered with its own calibration file
- Gain changes with overvoltage (V_{OP}≈54V @ 25°C)
- Temperature coefficient: +54 mV/°C:

V_{OP} (@ -50°C) = V_{OP} – (0.054 V x 75)

Electronic readout scheme



ANALOG SIGNALS **DIGITAL SIGNALS**

FEB (Front End Board)

inside the cryostat

- 4024 tiles, 4024 FEBs
- 2 channels on 1 FEB/tile
- Total 8048 channels
- Analog signals from FEB transferred to FEC via differential pairs, ~ 4 m inside the SS tank, ~14 m outside the tank

FEC (Front End Controller)

outside the cryostat

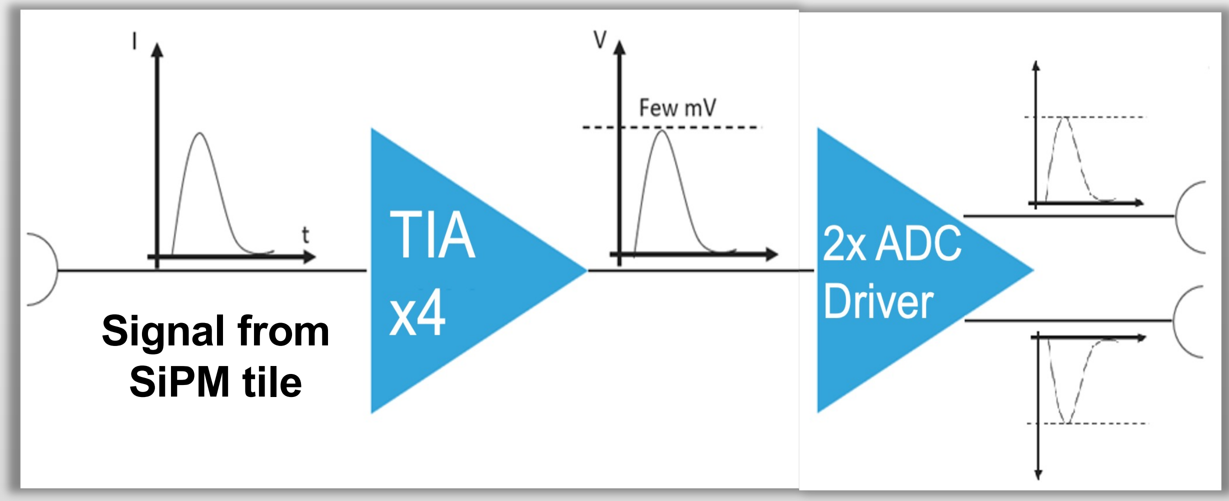
- 258 ADC boards --> 66 FECs
- ADC is on FEC, used to digitize analog SiPM signals from the FEBs
- FPGA & Power boards in μTCA.4 crate
- Q/T information is extracted with FPGA (waveform analysis)

Front-End Boards

Planar version with aramid PCB

2 stage amplifier:

TransImpedance Amplifier + Differential Driver



Differential pairs to FEC

LTC6268

500 MHz Ultra-Low Bias Current FET Input OpAmp

A_1 = 8.2 kV/A

LTC6405

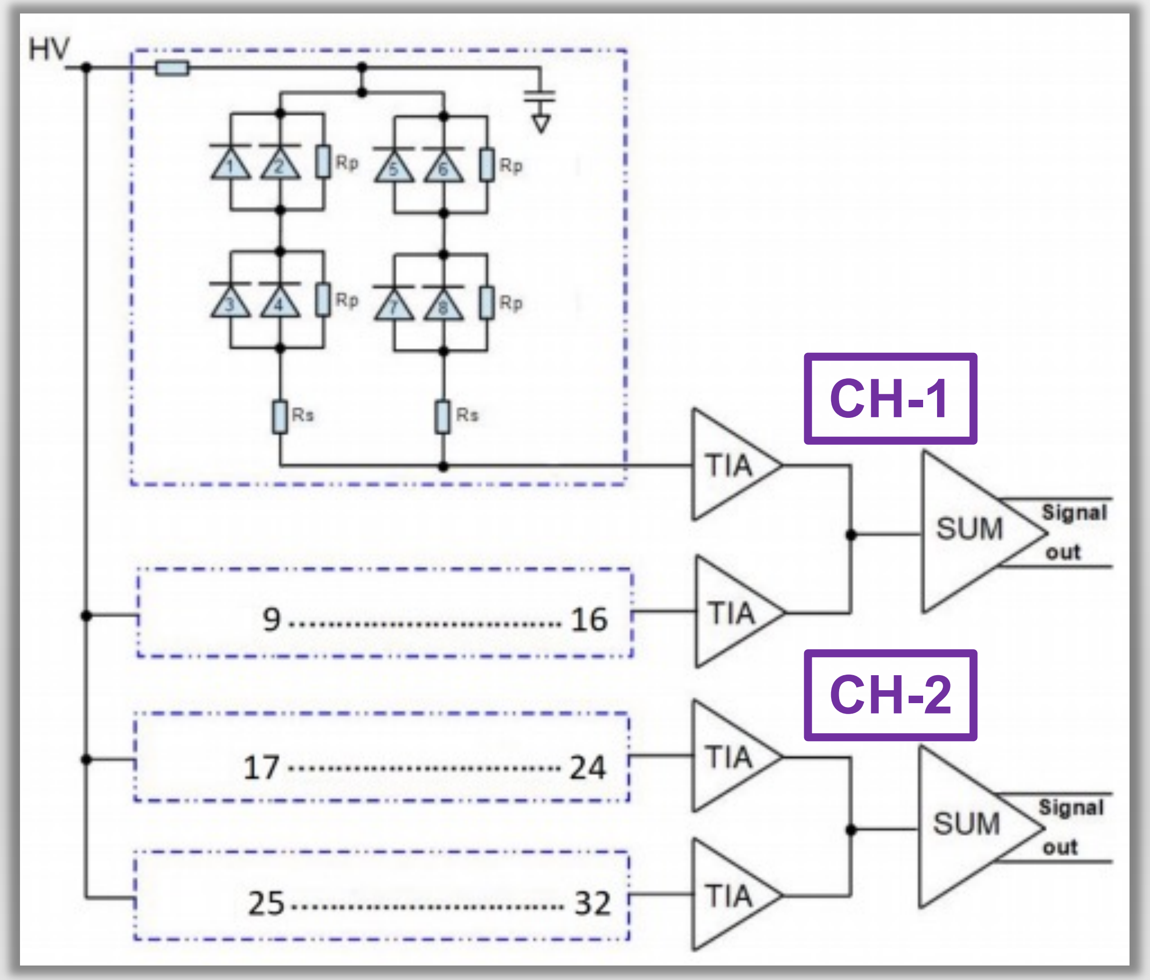
Low Noise, Rail-to-Rail Input Differential Amplifier/Driver

A_2 = 1.95 V/V

OVERALL GAIN: $A_1 \times A_2 \approx 16k$ [V/A]

The 32 SiPM elements of each tile are splitted in 4 TIAs

series of 4 SiPMs connected in parallel



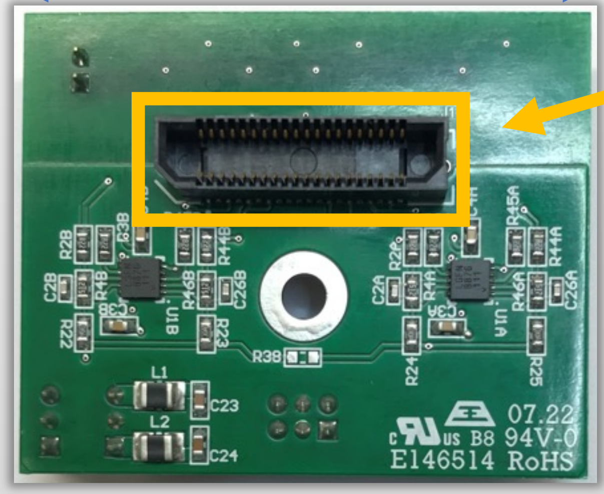
Front-End Boards

Planar version with aramid PCB (low background)

2 stage amplifier: TIA + differential driver

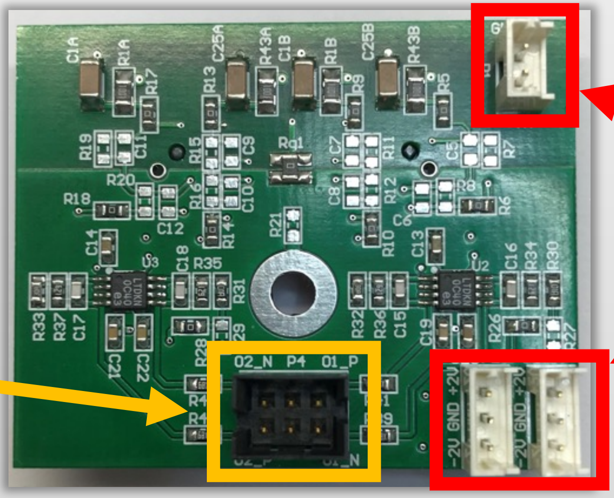
5 cm

3 cm



SiPM Tile
Board-to-board mating

Signal output
Differential pairs



HV SiPM
supply ≈ 2x50 V

LV FEB
supply ±2.2 V

FRONT: INPUT + 1st STAGE

REAR: 2nd STAGE + OUTPUT

- Single p.e. amplitude ≈ 10 mV ➡ p.e. channel dynamic range: 1–125 p.e.
- FEB needs ±80 mA at +2.2V and -2.2V @ -50°C ➡ 0–2V linearity range
- Shaping time ≈ 500 ns
- Recovery time < 1 μs
- SiPM gain adjustment with overvoltage ($G \approx 4x10^6$ @ V_{OP})

Flanges Cabling

- In order to decrease the number of the cables, and try to simplify the connections, there are 8 flanges with 8 signal pcb boards and 2 power supply pcb boards each.

INSIDE CRYOSTAT – To FEBs

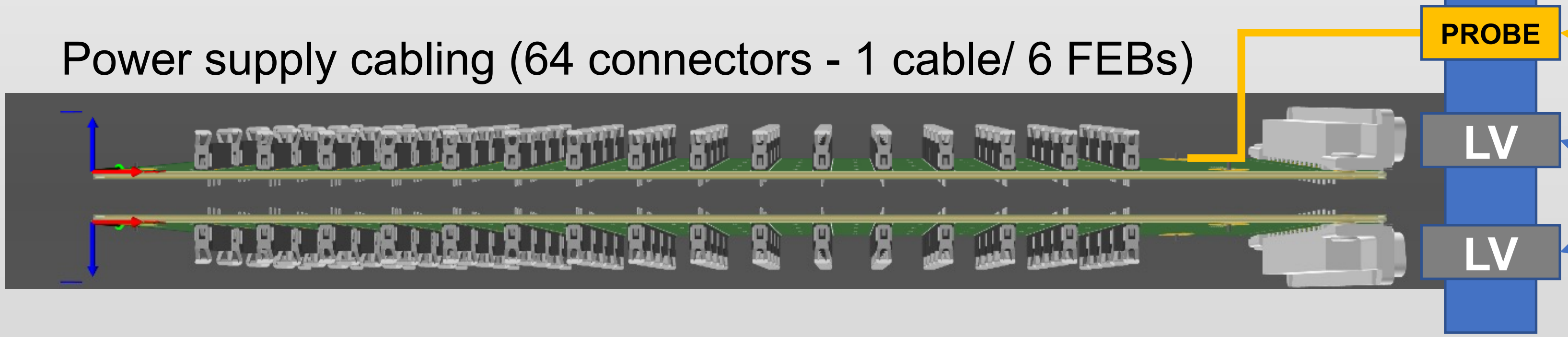
Inside cables length ≈ 3m

Signal cabling (64 connectors - 1 cable ~3m/FEBs)

OUTSIDE CRYOSTAT

To FEC/ADC boards
(16 differential pairs x 8 connectors)

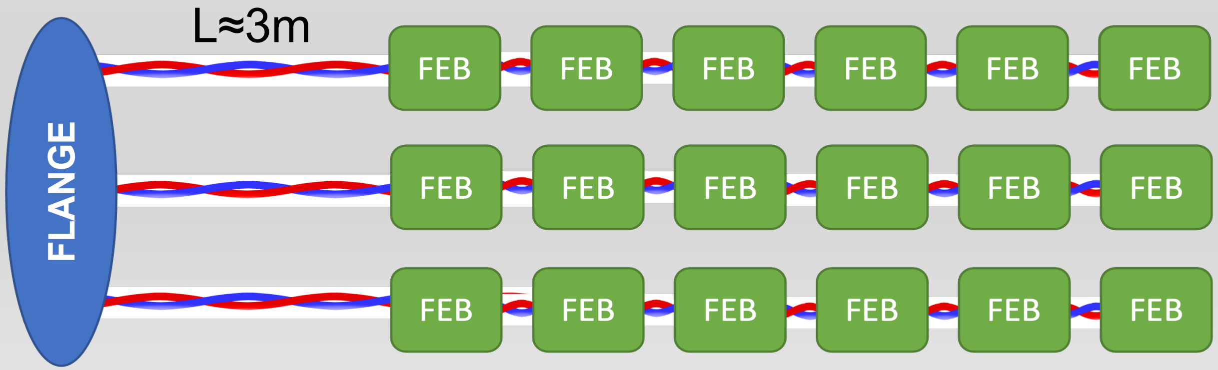
Power supply cabling (64 connectors - 1 cable/ 6 FEBs)



9 pin DSUB connector for V/I monitoring

25 pin DSUB connectors from LV power supplies

Outside cables length ≈ 14m



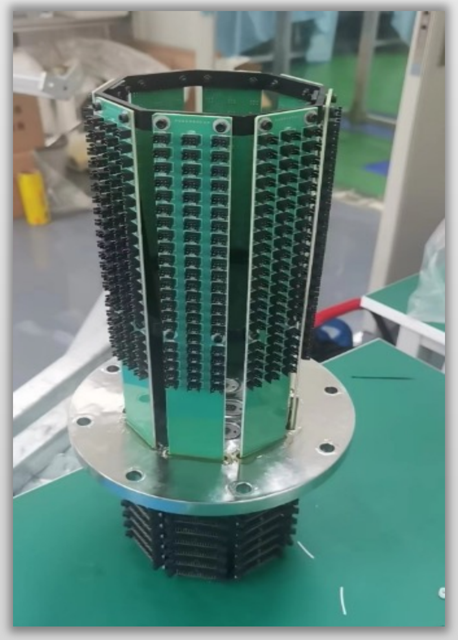
- Each flange have to supply 512 FEBs
- FEBs can be subdivided in ~86 rows with 6 FEBs each
- 86 long pairs (~3m) come from the flange to the first FEB of each FEB rows
- 5 shorter cables (~15cm) can be used to bring supply to the other FEBs on each row

1:1 TAO Prototype

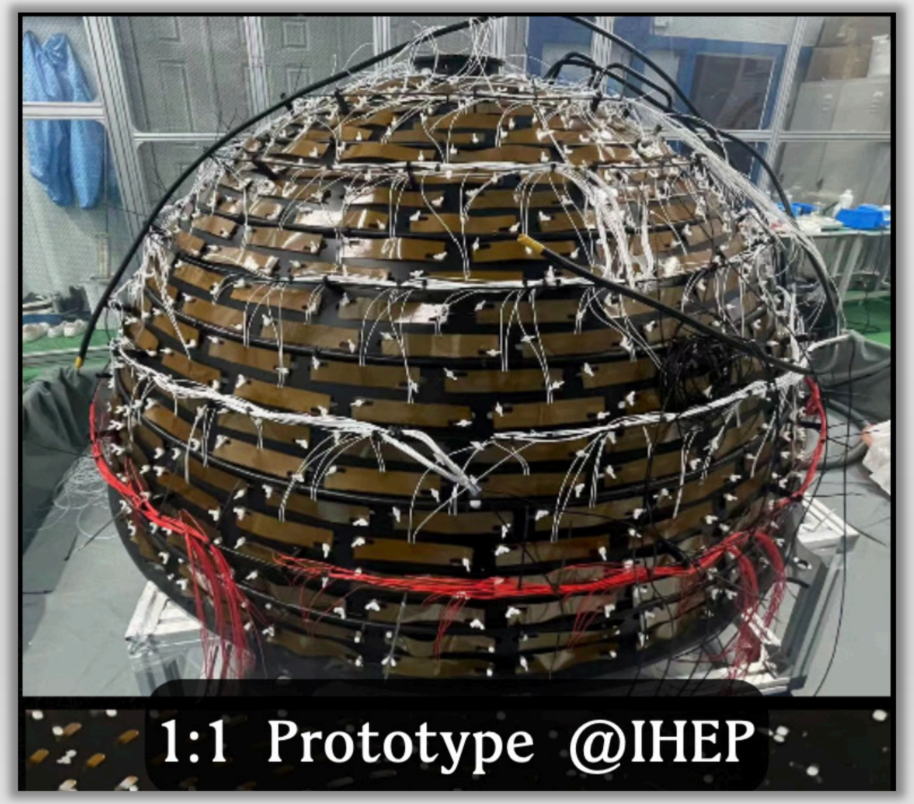
The TAO detector 1:1 prototype is under construction in Beijing at IHEP (Institute of High Energy Physics)

- ❑ Test key installation procedures before the transfer to the Taishan Nuclear Power Plant in Guangdong
- ❑ The aim is avoiding big issues and save time on site (i.e.: copper shell rotation, SiPM assembly, cabling, tools)
- ❑ Test performance of cryogenic system, FEBs with SiPM tiles (~100), LS, calibration system, etc..

Pre-production FEB batch



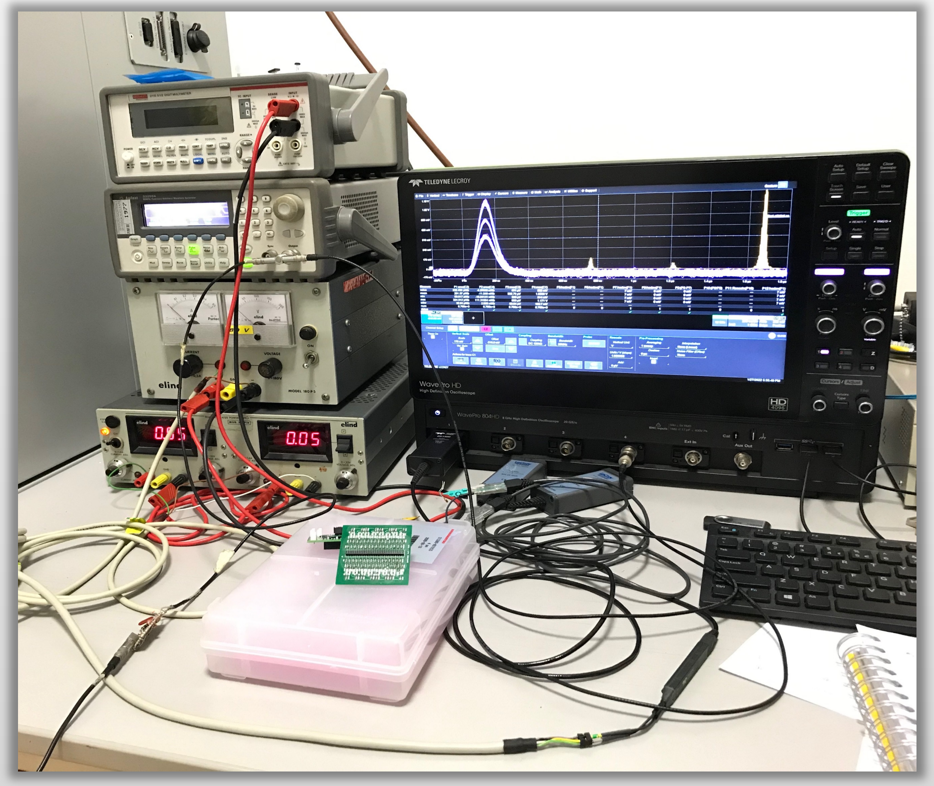
Assembled flange
signal + power boards



Experimental setup

Tile characterization performed @ -50°C (in dark condition or laser source)

CLIMATE CHAMBER



SUPPLY & READOUT

- Low-Voltage power supply
- High-Voltage power supply
- 407nm-80ps LASER source
- LeCroy WavePro Oscilloscope

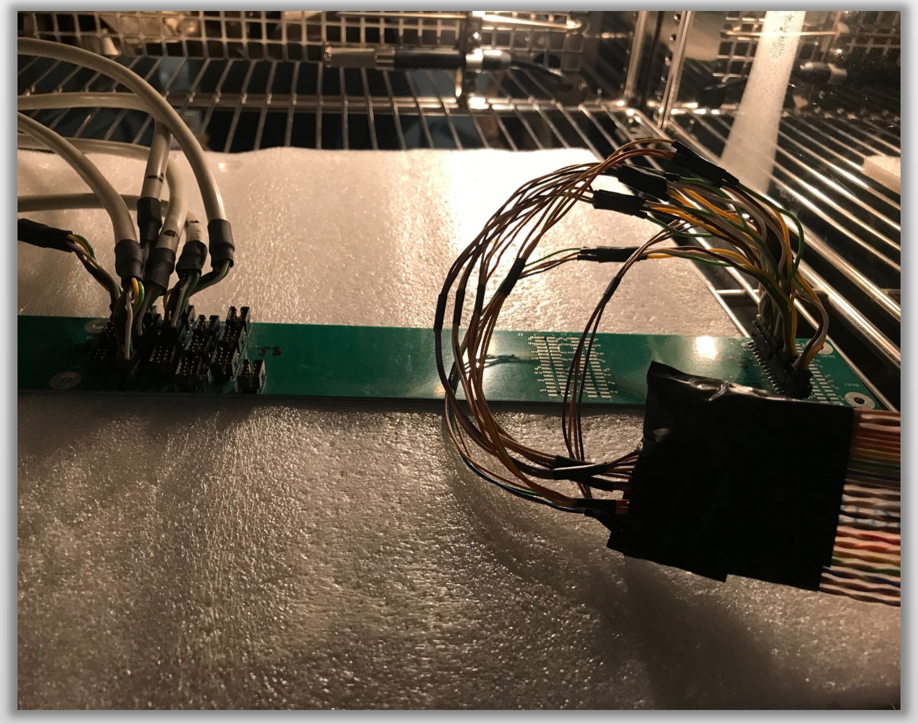
6 FEBs + Tiles tested at one time – 12 overall channels

FEBs LV (2V) supply on the row
$I_{LV\text{-}BIAS}$~80mA x $\#_{FEB}$ @-50°C

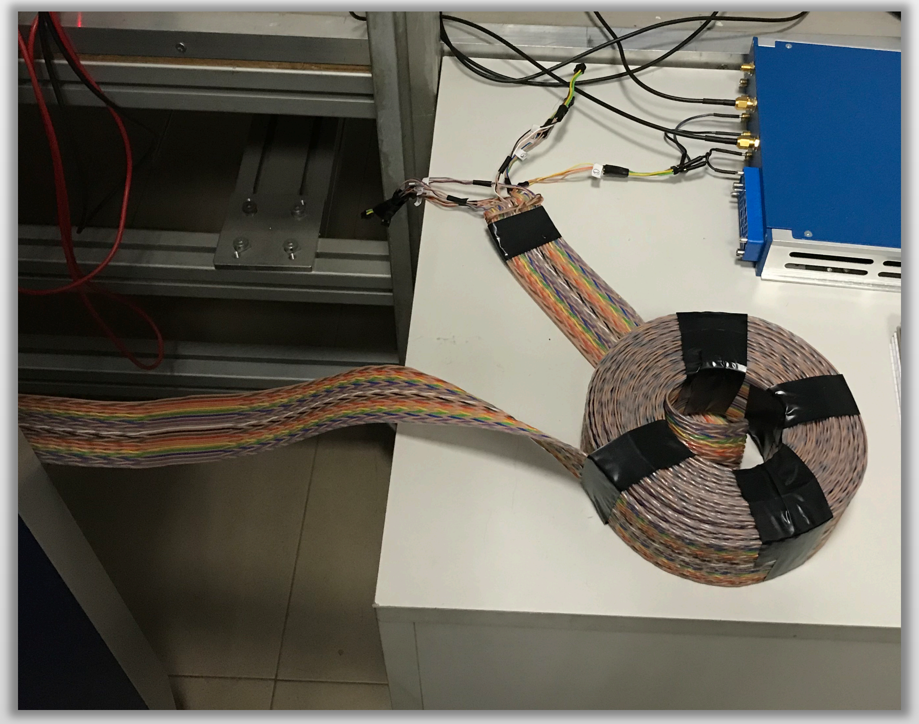
High-Voltage power supply (≈100V) splitted for all 6 tiles

FEBs supply & connection

6x 3m output connectors with flange and 14-meter twisted differential pair cable



Inside climate chamber

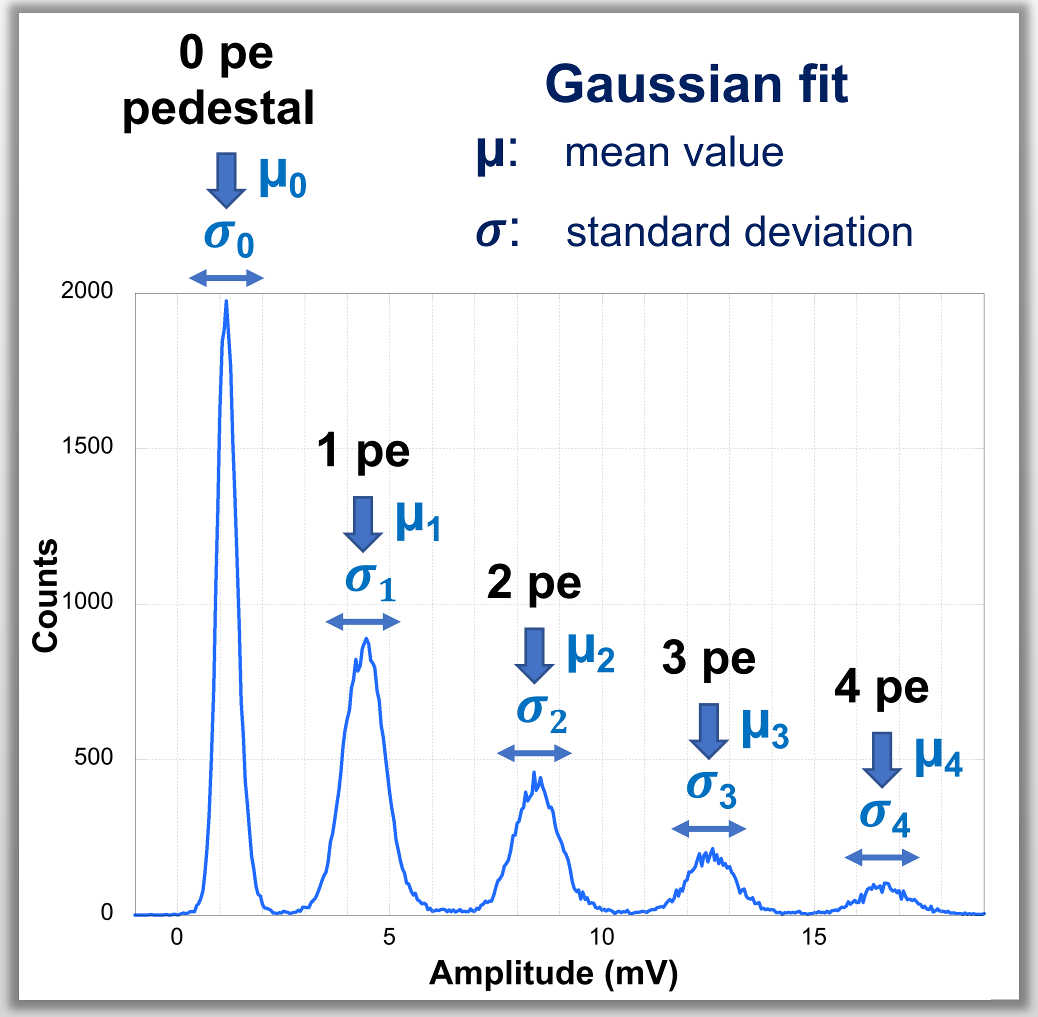


Outside climate chamber

Differential signals recombined by means of a transformer

(mismatched impedance: $50\Omega_{OUT}$ // $50\Omega_{IN}$ Oscilloscope DC-coupling)

CDR Figures of Merit



Maximum Histogram
4 photoelectrons + pedestal (zero)

4 figures of merit with specific requirements

(TAO CDR 2020/5/17)

LASER / DARK

- **Signal-to-Noise Ratio**

$$SNR = \frac{\mu_1 - \mu_0}{\sigma_0} \geq 10$$

- **Single PhotoElectron Resolution**

$$\text{RES} = \frac{\sigma_1}{\mu_1} \times 100 \leq 15\%$$

DARK

- **Crosstalk**

$$\text{XTLK} = \frac{N_{2+}}{N_1} \times 100 \leq 20\%$$

- **Dark Count Rate**

$$\text{DCR} = N_{1+} \leq 100 \ [\text{Hz/mm}^2]$$

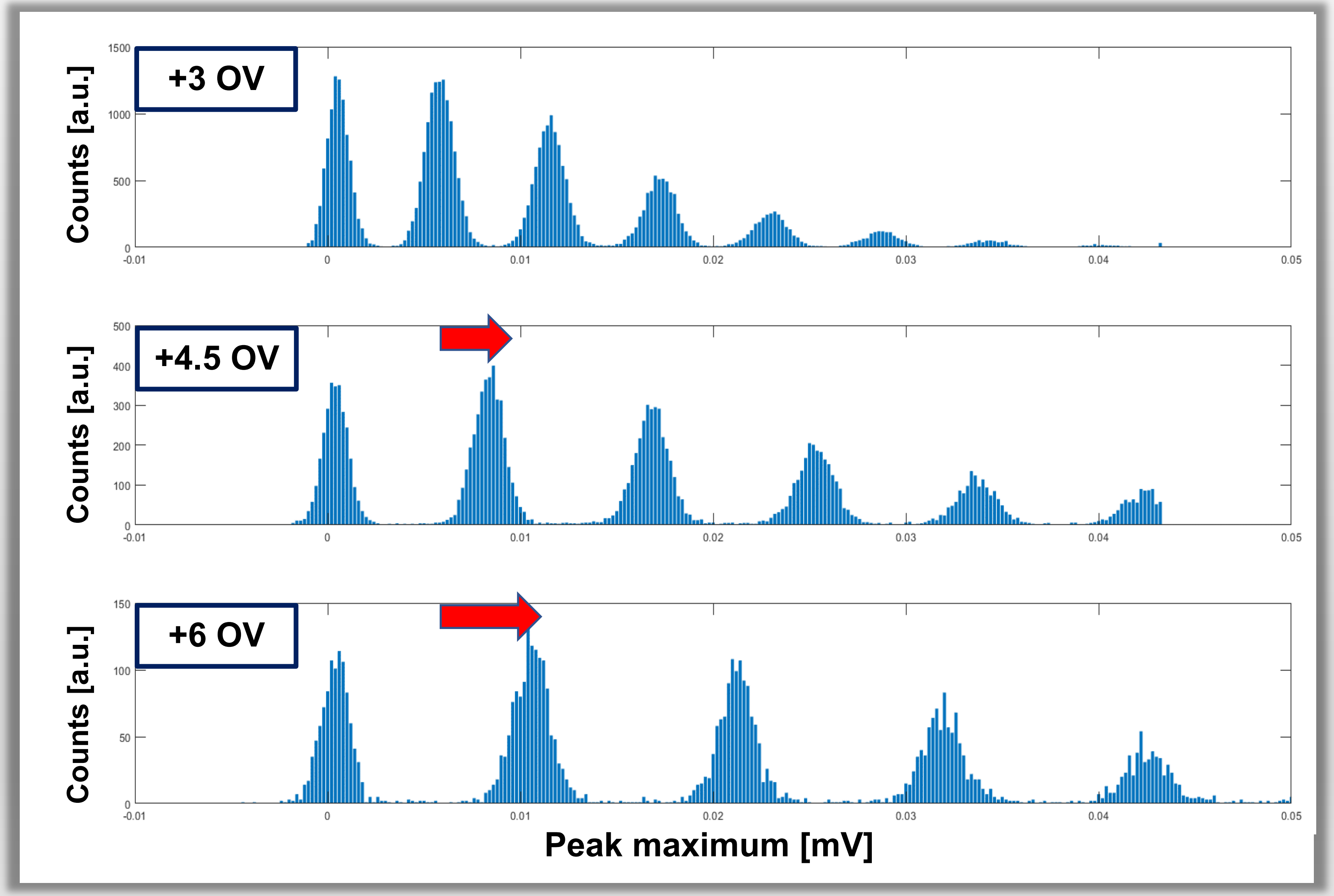
Dynamic Range requirements

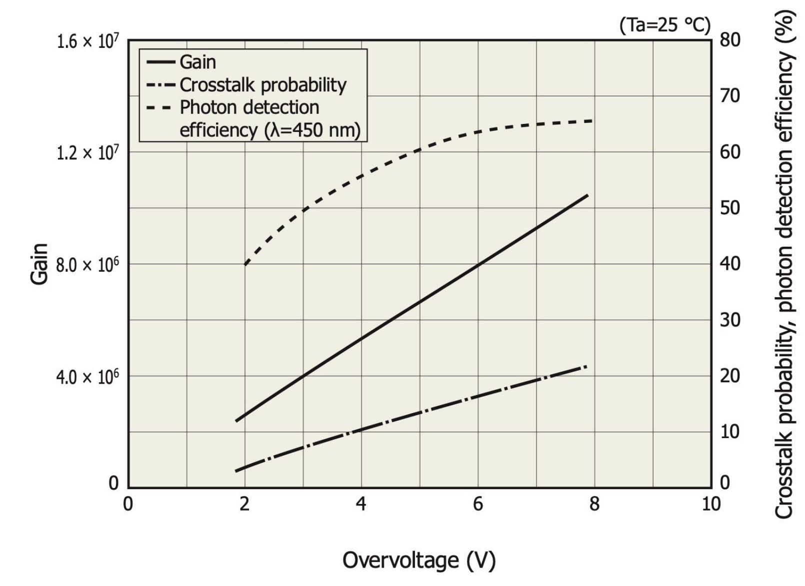
- Single P.E. maximum amplitude ~ 15 mV
- 0V-2V output linearity range *(compatible with ADC input range)*
- P.E. Channel dynamic range 1 – 125 p.e. (1–250 p.e. on the whole tile)
- Recovery time < 1 µs

✓ $\mu_{k+1} - \mu_k \approx 8$ mV @ $V_{OP} = +3$V OV
✓ Shaping time ≈ 500 ns
- p.e. amplitude, SNR, RES adjustments with overvoltage

SiPM Overvoltages

Effects on the SiPM tile for different Over Voltages (V_{OP} = +3V OV)





- ✓ Single Electron (S.E.) resolution & Signal-to-Noise Ratio increasing
- × Crosstalk increasing
- × Dynamic Range decreasing

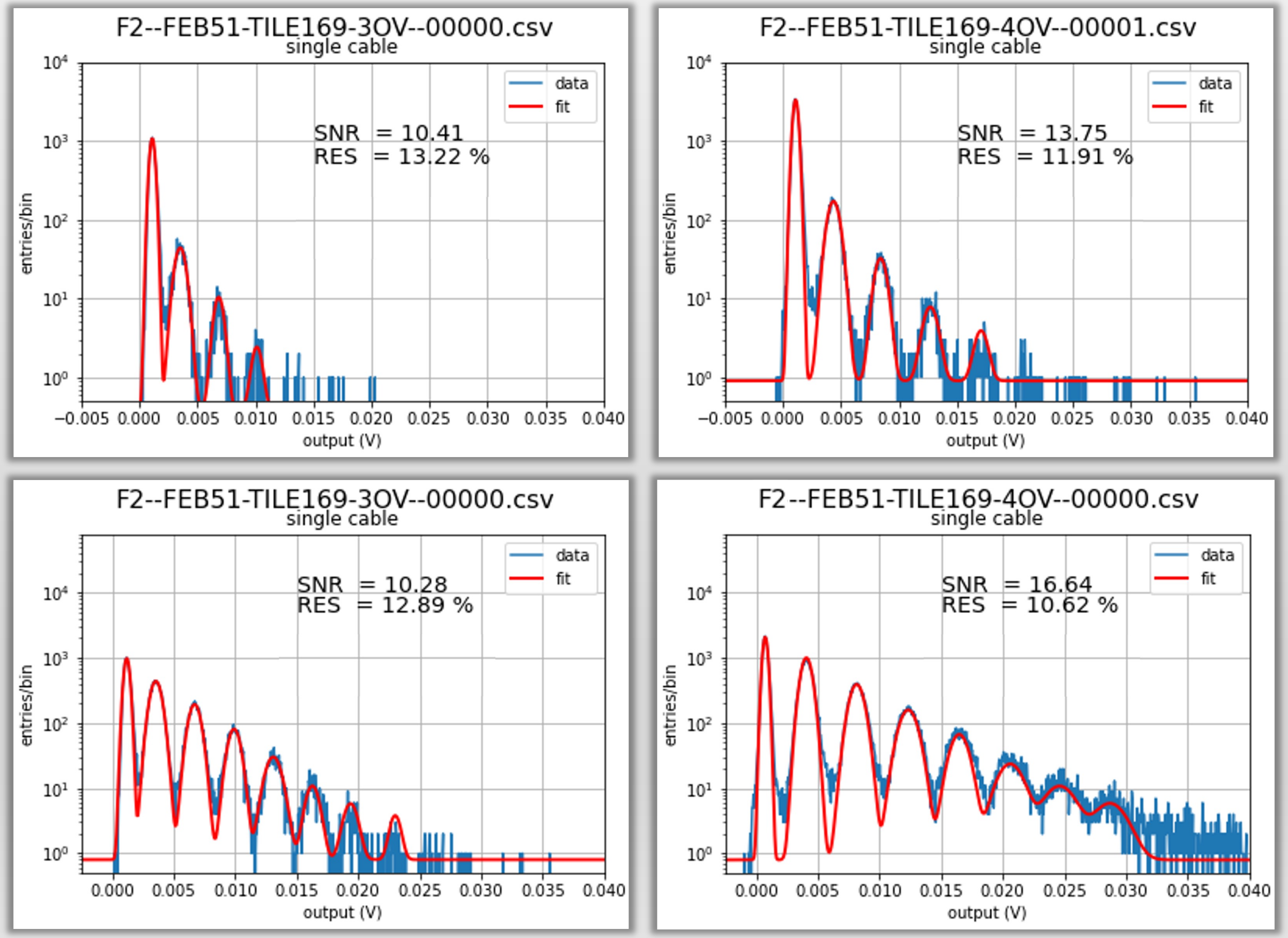
Tiles Characterization

100 pre-production FEBs tested with pulse electrical source (linearity, gain) and with SiPM tiles, in dark condition and with a very-low intensity laser source (λ=407nm) @ -50°C (RES, SNR, DCR)

+ 3V OV **+ 4V OV**

DARK

LASER



- **RES, SNR, XTLK: Gaussian fit over maximum histograms**
- **DCR: Count of events above a voltage threshold (halfway 0 and 1 p.e.) normalized with 1s and overall area (12x12 mm² x8, half-tile). About the same for all FEBs and Tiles, and in datasheet range:**

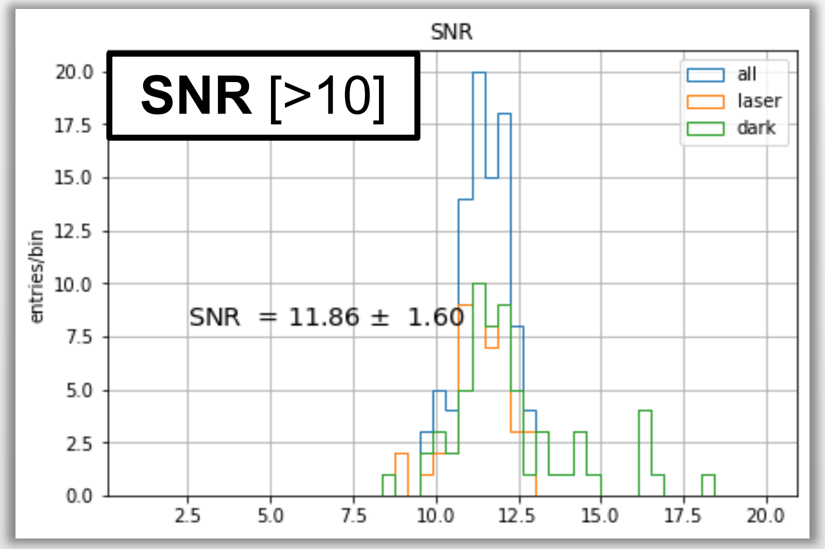
➡ ~25 [Hz/mm²] @ +3V OV

➡ ~32 [Hz/mm²] @ +4V OV

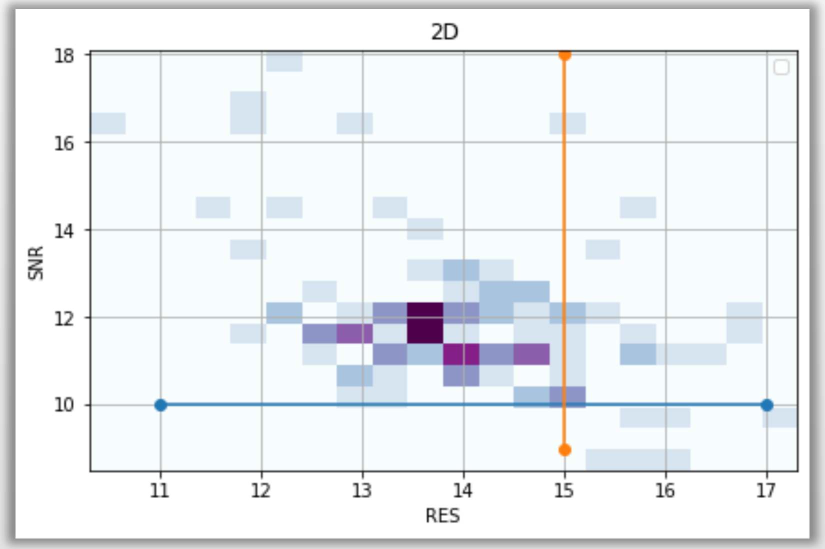
Typ. 2000 / Max. 6000 (Typ. 13.9 / Max. 41.7)	cps/ch. (cps/mm²)

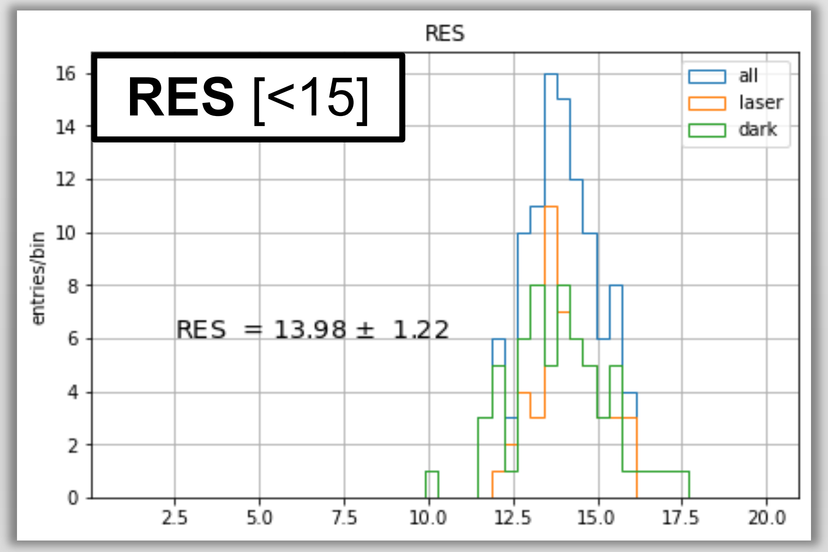
$DCR_{@25°C} \approx 4000 \times DCR_{@-50°C}$

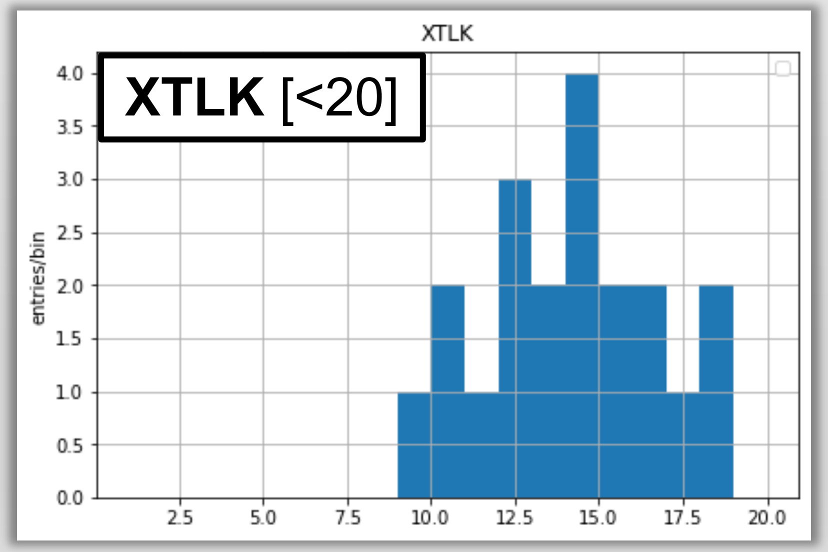
Characterization summary @ +3V OV



SNR vs RES







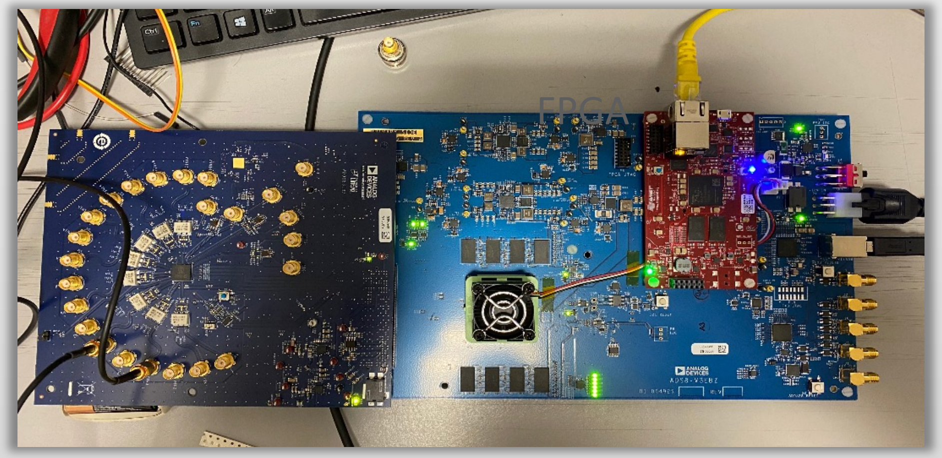
- **RES, SNR, DCR and XTLK: expected results as the requirements**

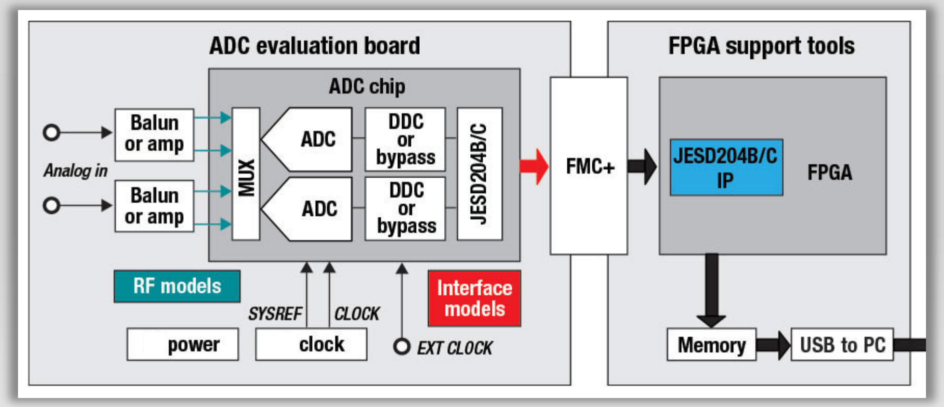
ADC Board Prototype

Analog Devices – ADC demo-board

(for preliminary test)

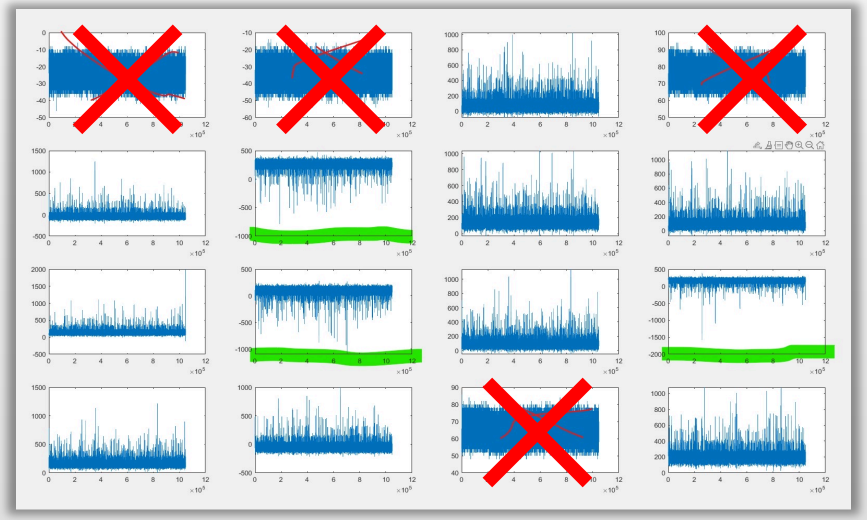
- **AD9083EBZ** evaluation board
- **ADS8-V3EBZ** Data Capture Board
- FPGA controller (Kintex7)
- Ethernet connection with PC



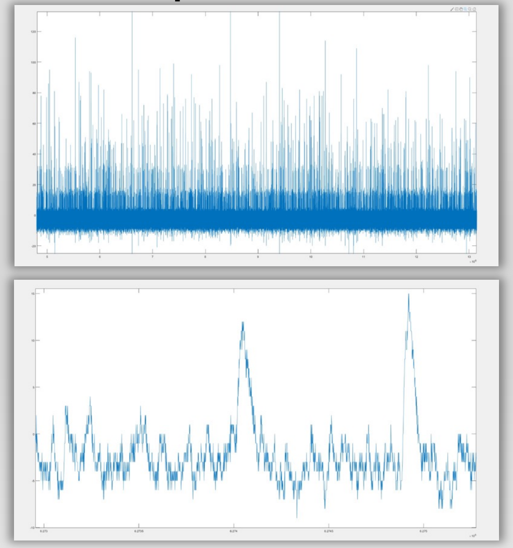


All 16 channels readout at one time

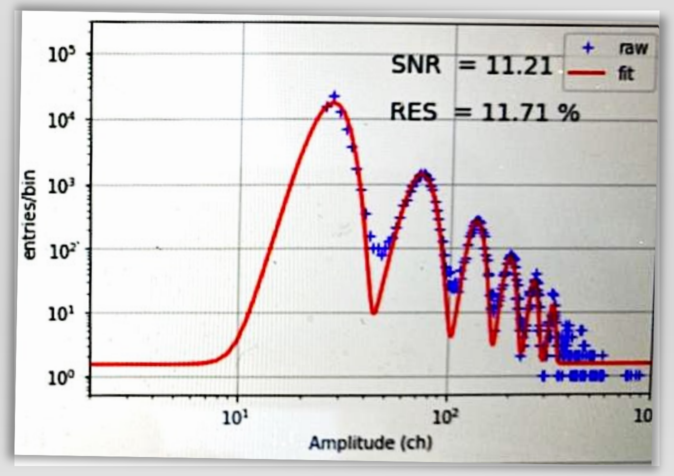
(6 FEBs connected - only 12/16 active channels)



Acquired data

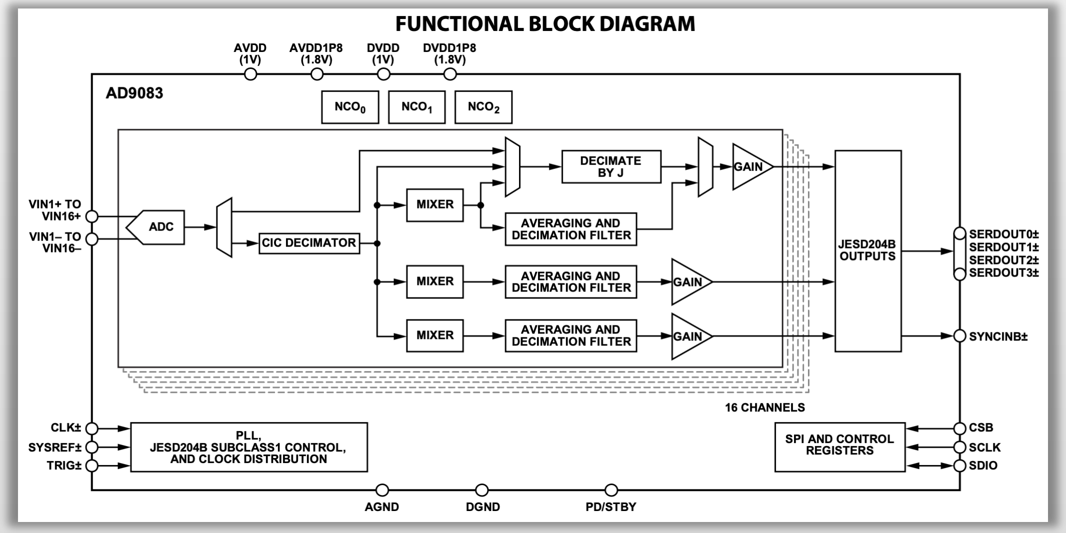


Reconstructed histogram



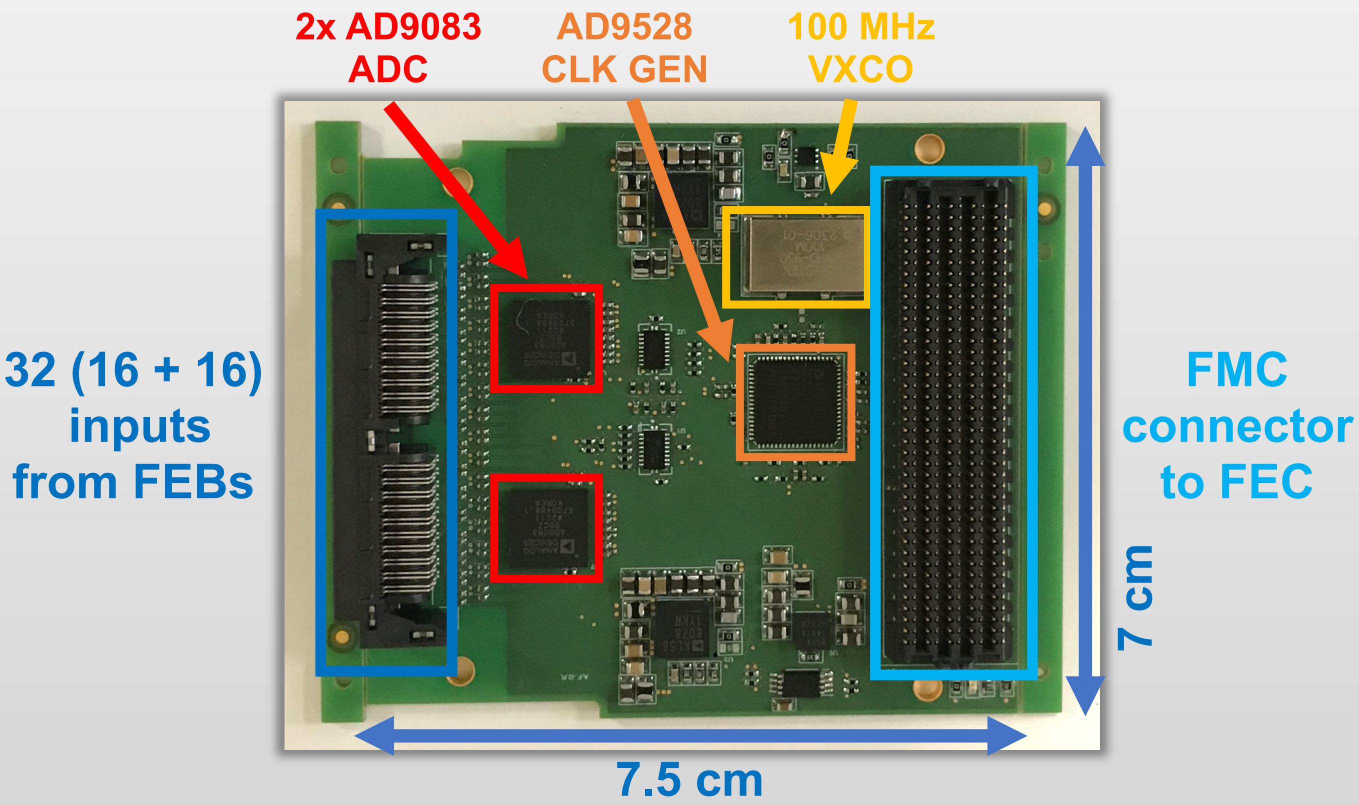
ADC Board Prototype

Custom ADC board (7.5 x 7 cm^2) with 2 AD9083
32 input differential channel per board, accessible by FMC connector



AD9083

- ∑-∆ analog-to-digital converter (ADC)
- 125 MHz usable analog input bandwidth
- Sample rate up to 2 GSPS
- 16 input channels
- 4 JESD204B Subclass 1 encoded outputs
- Differential input (0.5 to 2 V_{PP})
- Digital processor
- 1.0 V and 1.8 V supply operation



- 250 MSample/s ADC,125 MHz bandwidth
- 32 channels - Differential input 2 V_{PP}
- Dedicated Input for shared clock between different board
- FMC connector for power supply and output signals

ADC Board Prototype

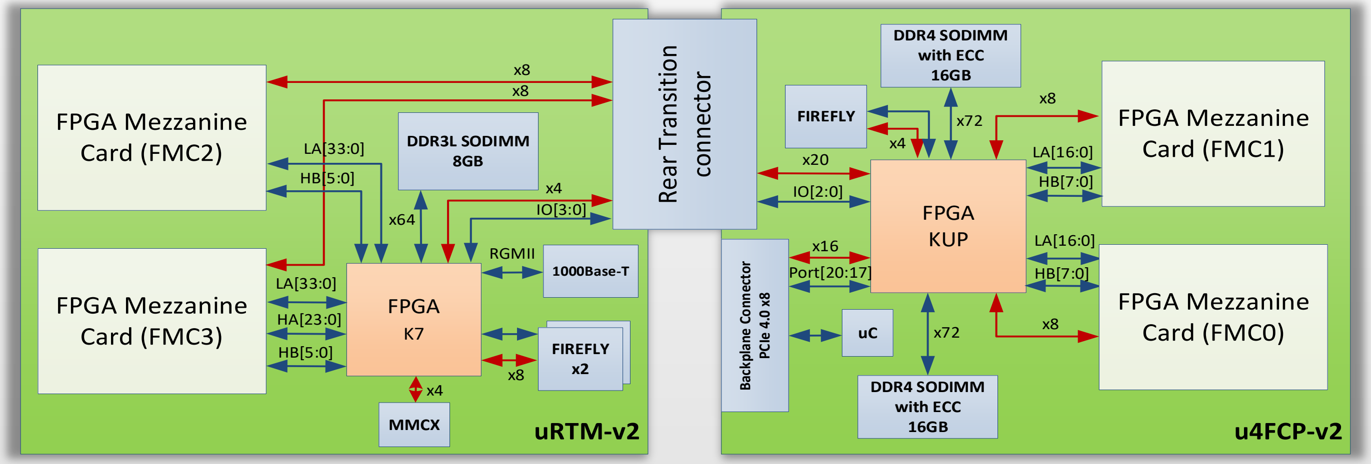
STATUS OF WORKS

- 2 ADC boards arrived last week
- They are currently under test for firmware debugging

- FMC pinout compatible with Analog devices ADC demo board and ADS8-V3EBZ (16 input channels reading at one time)

- Kintex7 FPGA-based Front-End Controller (FEC) has been developed at IHEP
- The FEC can control 4 ADC boards, for a maximum of 128 channels read at one time

- A dedicated trigger & DAQ system will filter and record occurring events, rejecting dark count events

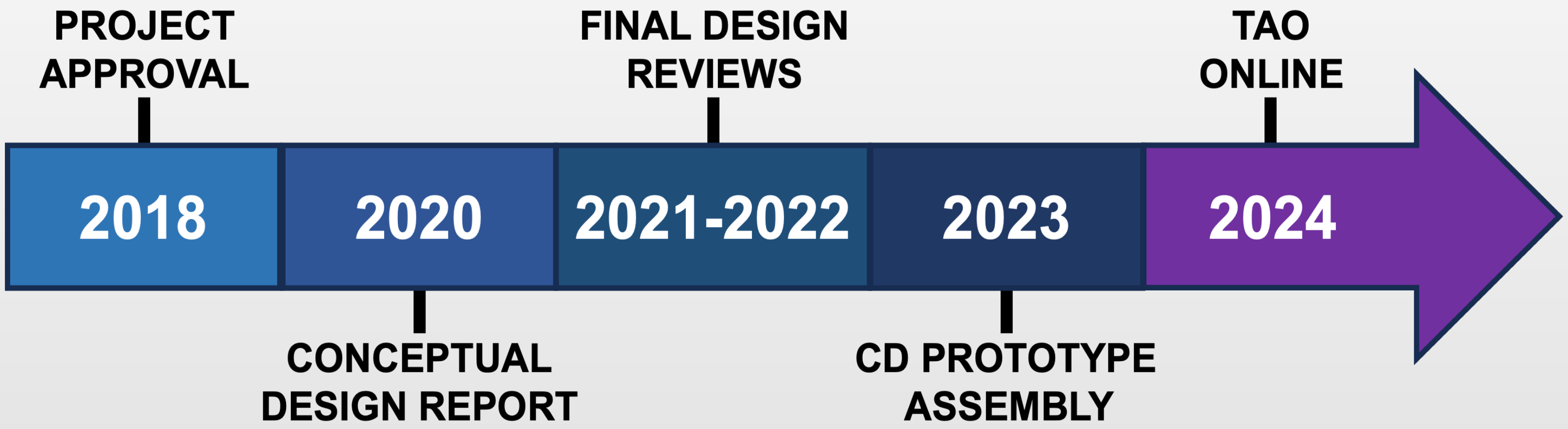


2x ADC BOARD

FEC BOARD
(IHEP)
max 128 channels

2x ADC BOARD

Conclusion



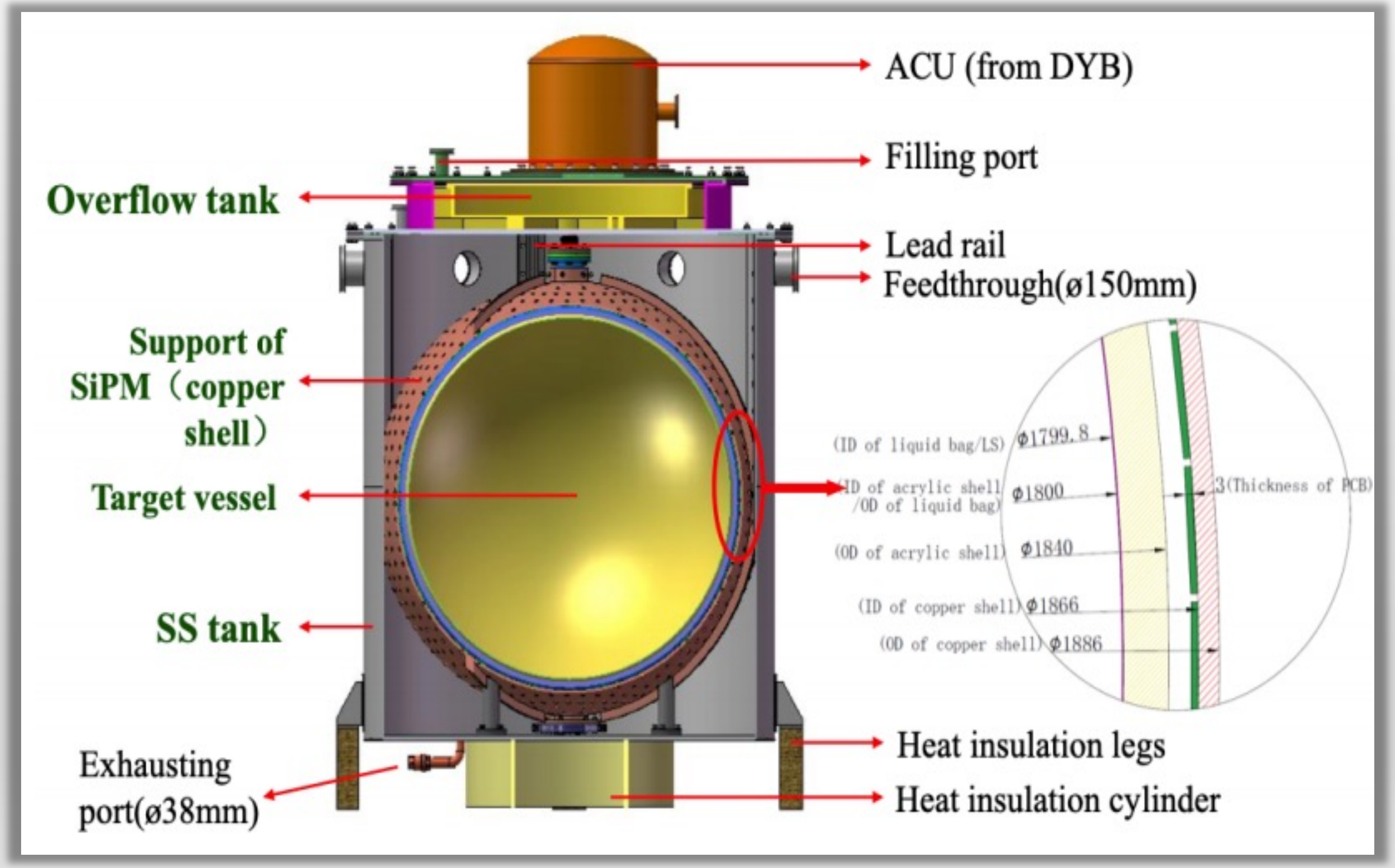
- High resolution measurement of the reactor antineutrino spectrum
- Design of the TAO readout front-end electronics reported
- Preliminary tests demonstrating the fulfillment of the TAO requirements
- Automatic data acquisition by means of ADC boards with FPGA controller
- JUNO-TAO: 1:1 prototype ready at the end of the 2023 and online in 2024
- Ready for the mass-production (waiting feedback from 1:1 prototype test)
- Custom board development for testing ~4000 FEBs (connections and gain)

Thank you for your attention

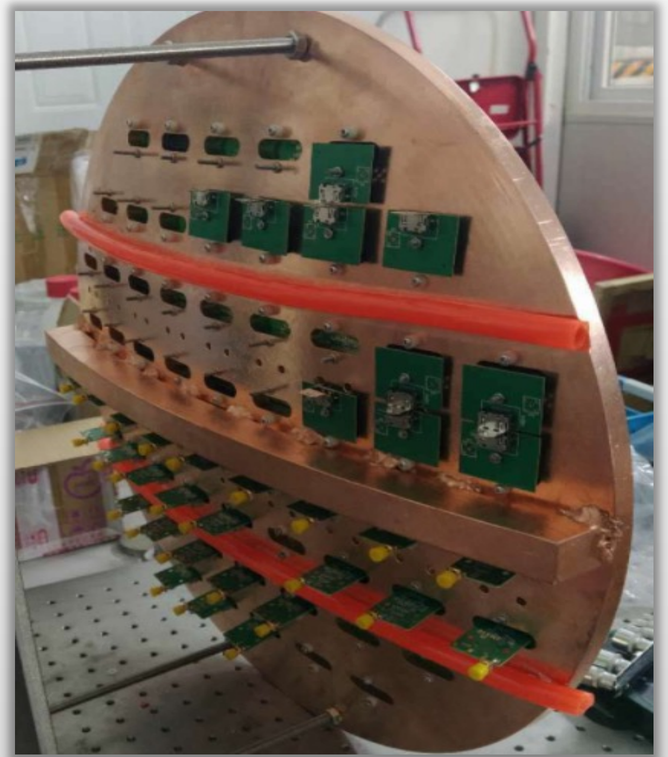
BACK-UP SLIDES

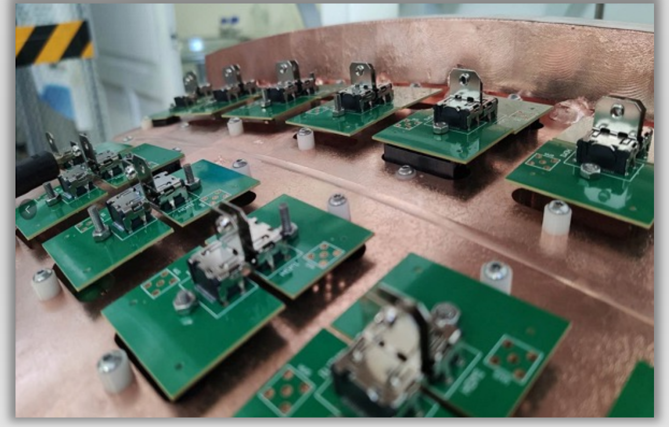
CD Overview

JUNO-TAO Central Detector (CD)



COPPER SHELL





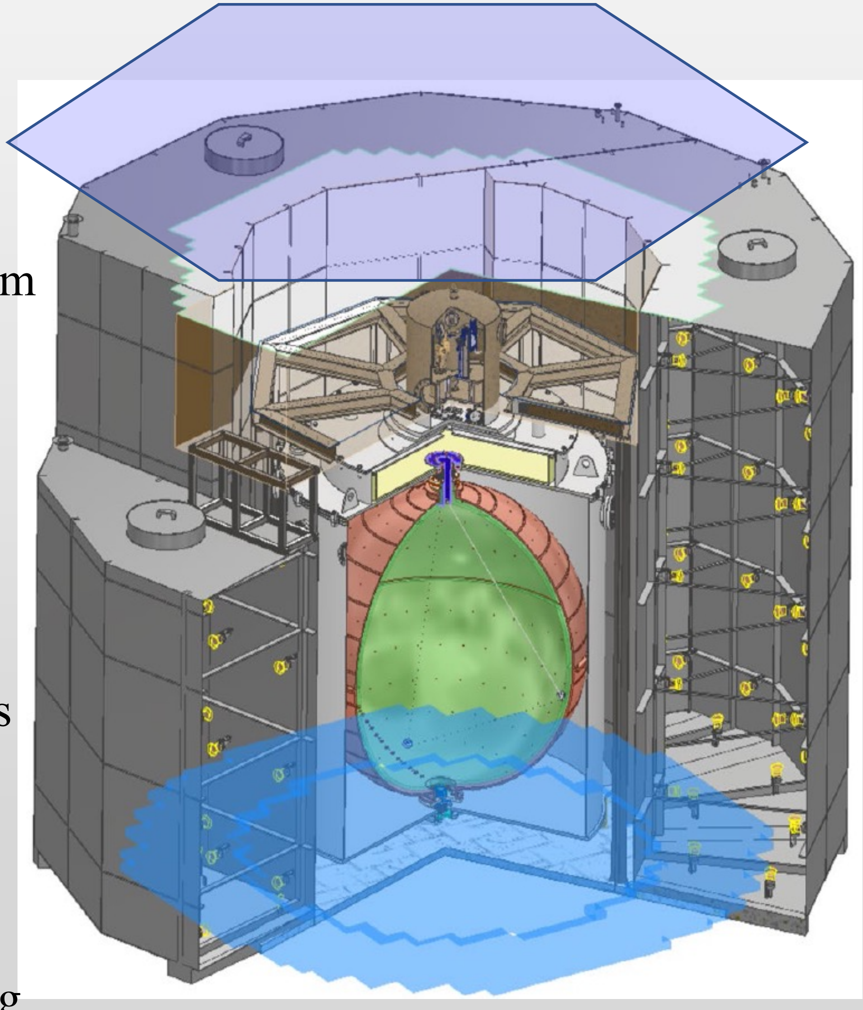
CD Overview

Highlights:

- Energy resolution <2%@ √E MeV
- SiPM PDE >50% (~4000 p.e./MeV)
- SiPM coverage: 94% of ~4π, ~10m^2
- SiPM DCR: <100 Hz/mm^2 @-50°C
- Dewatering Low-temperature LS : <10ppm

◆ Central detector

- **Acrylic sphere** 1.8m (ID), 20mm-thick with 2.8 t Low-T Gd-LS
- **Copper shell** 1.886m (ID), 12mm-thick with 4024 pieces of 50*50mm^2 SiPM tiles
- **SS tank** 2.09m(ID), 10mm-thick with 3.2 t LAB/Gd-LAB
- **Cryogenic system** with 4.5kW cooling power and 150mm-thick melamine foam full covering keeping -50°C running condition



◆ Top Veto Tracker (TVT)

4-Layer PS, 160 strips

2 m×20 cm×2 cm/strip

Top Shield(HDPE)

◆ ACU & CLS

6 types of exemption sources

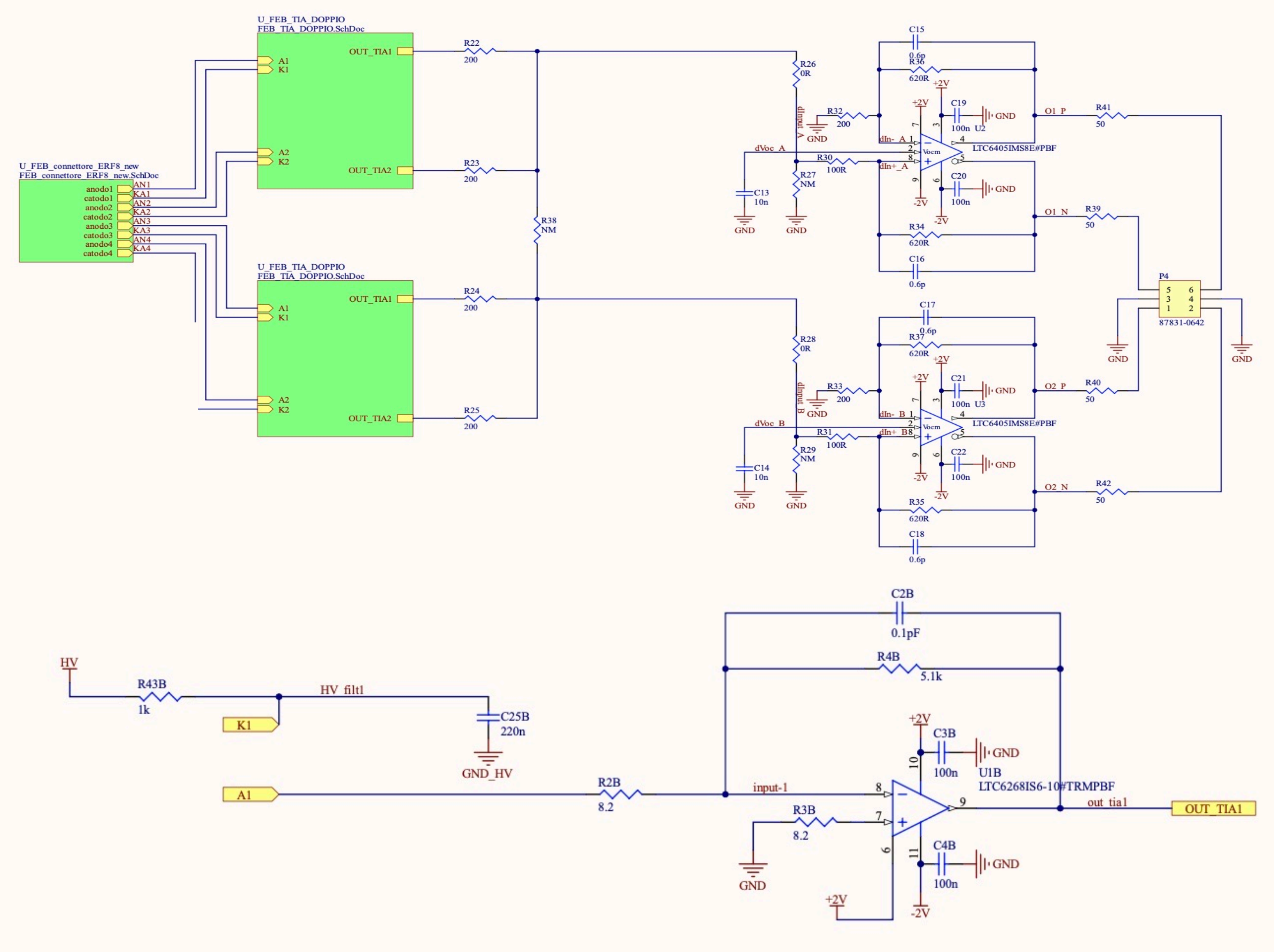
◆ Water Tank

3 irregular water tanks

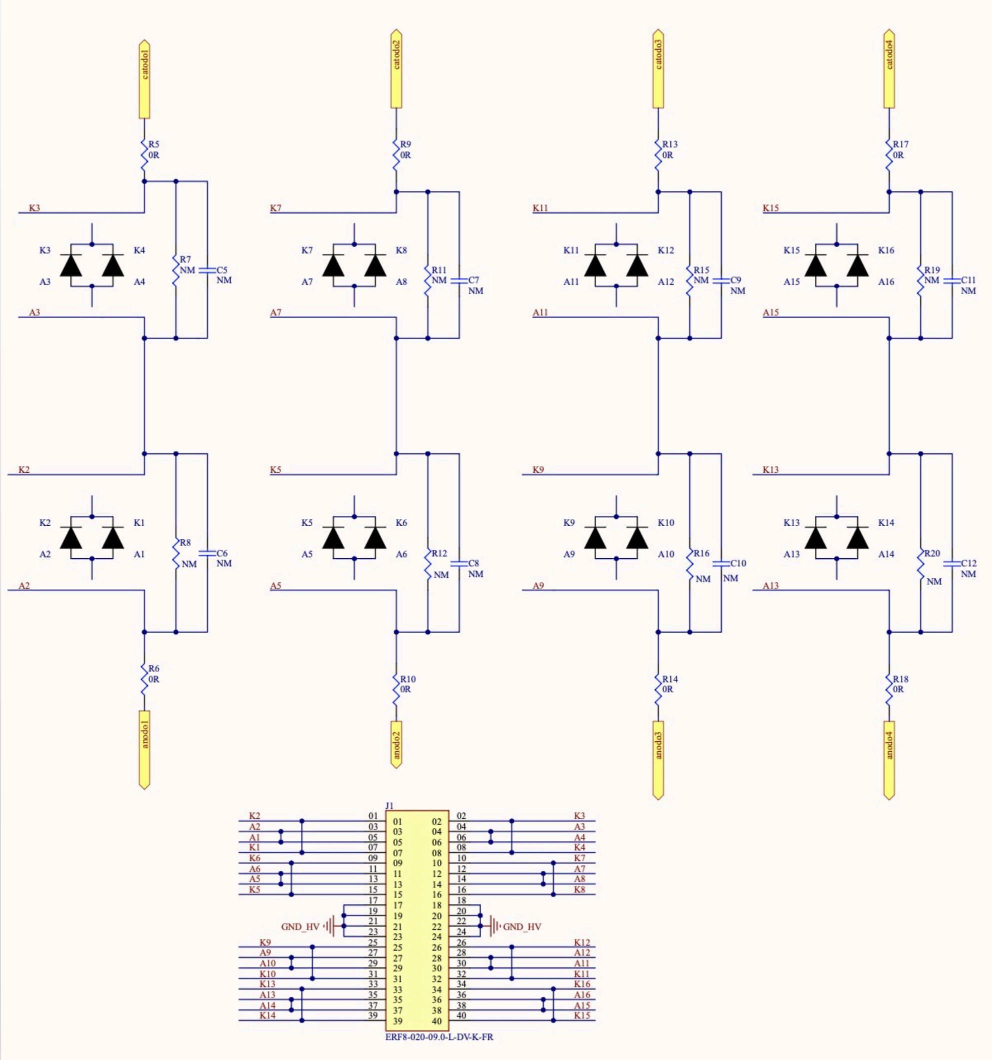
~300 3" PMT

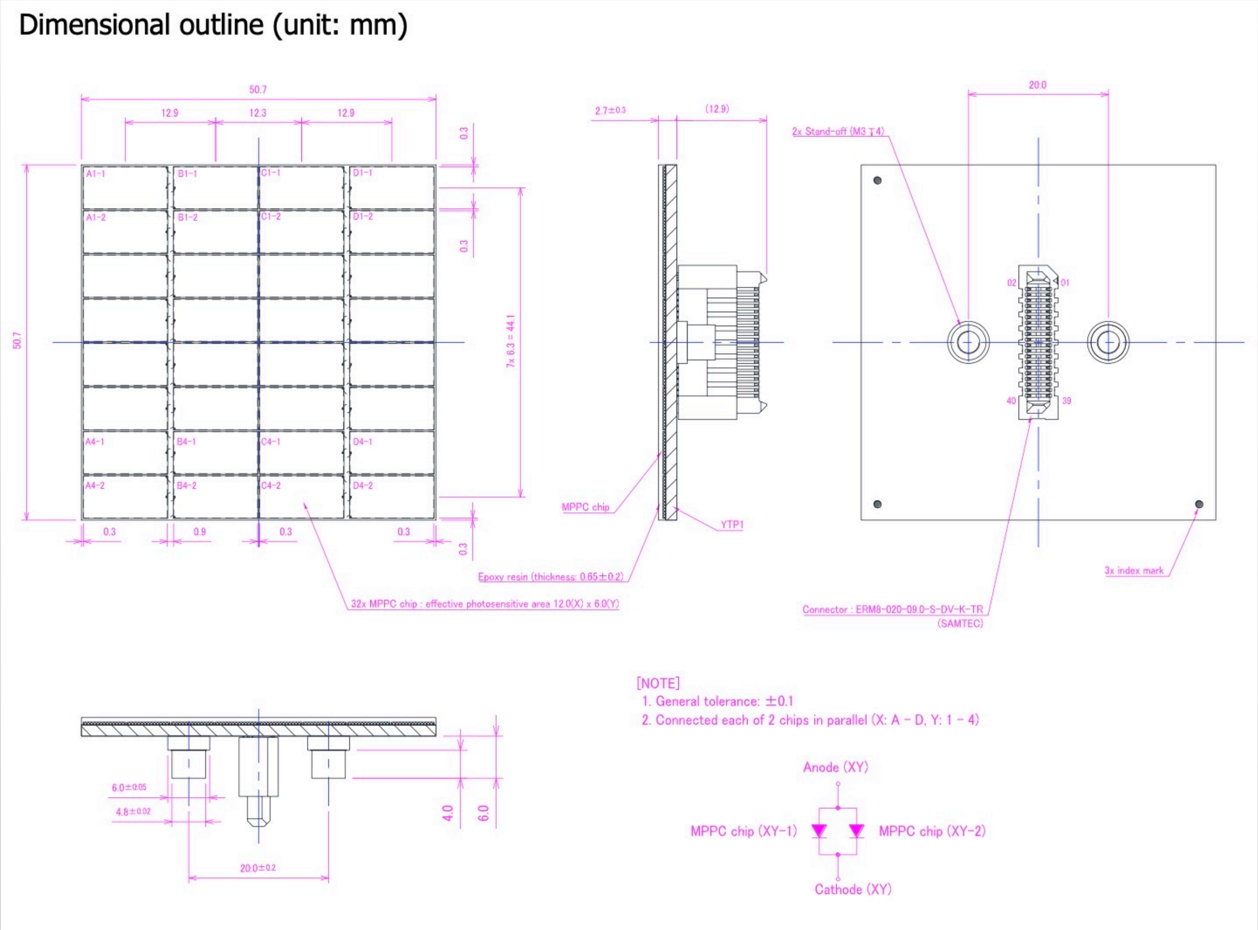
Overflow Tank
Cu Shell
SiPM Array
Acrylic Vessel
SS Tank
Insulation (MF) Bottom
Shield(Lead)

FEBs Schematics

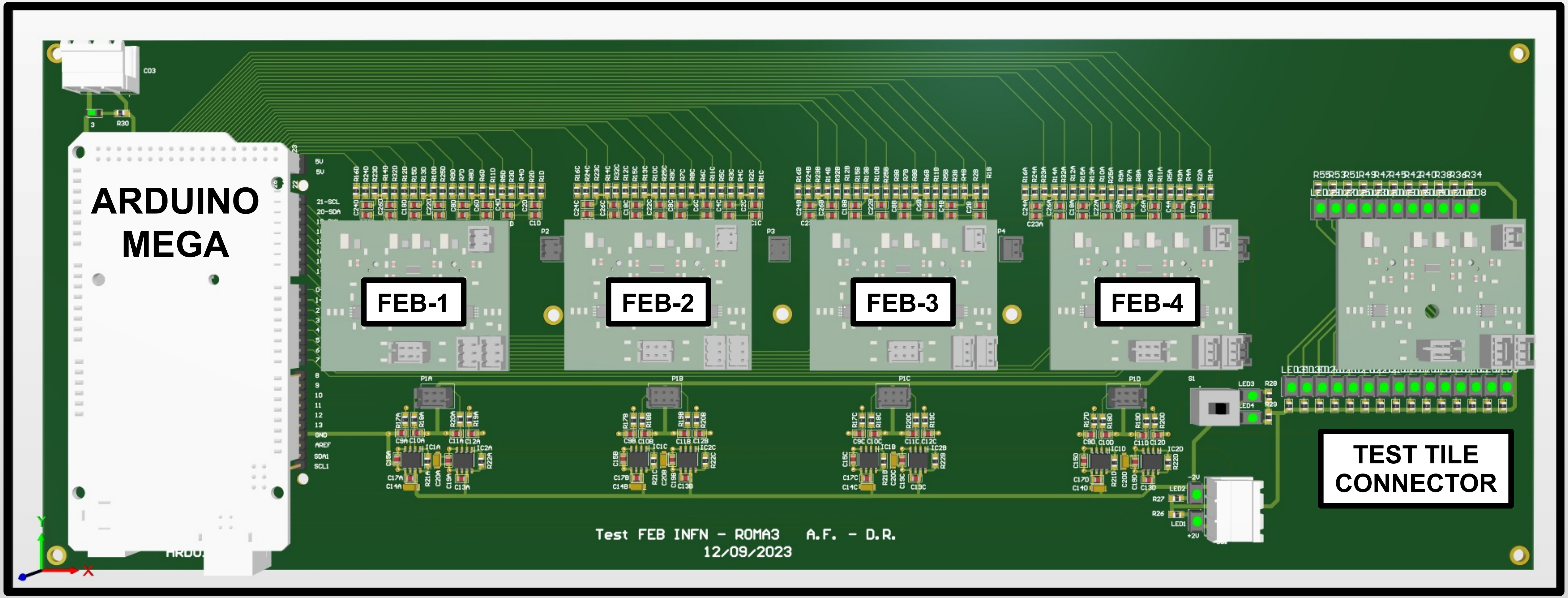


FEBs Schematics



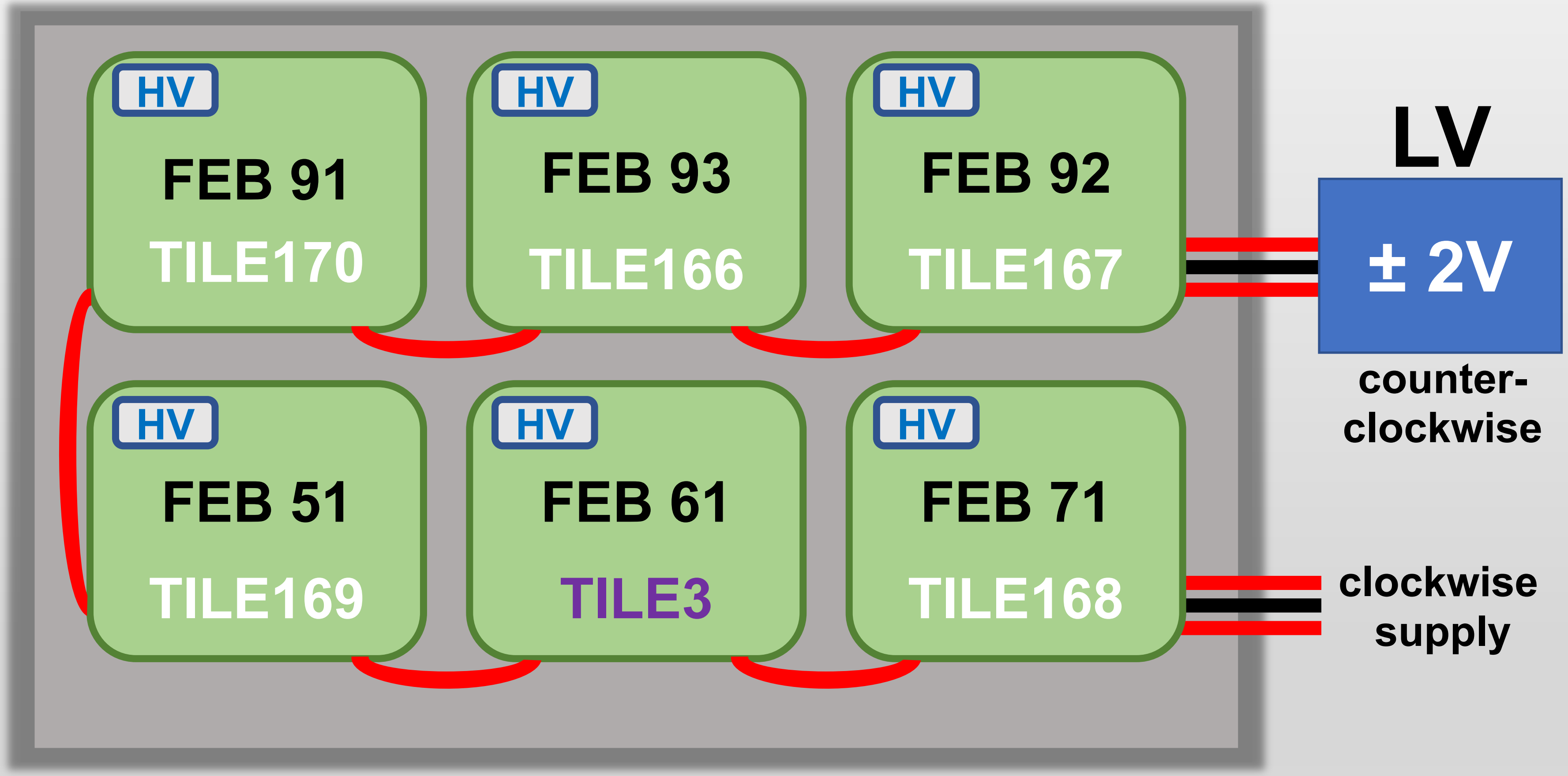


FEB Test Board



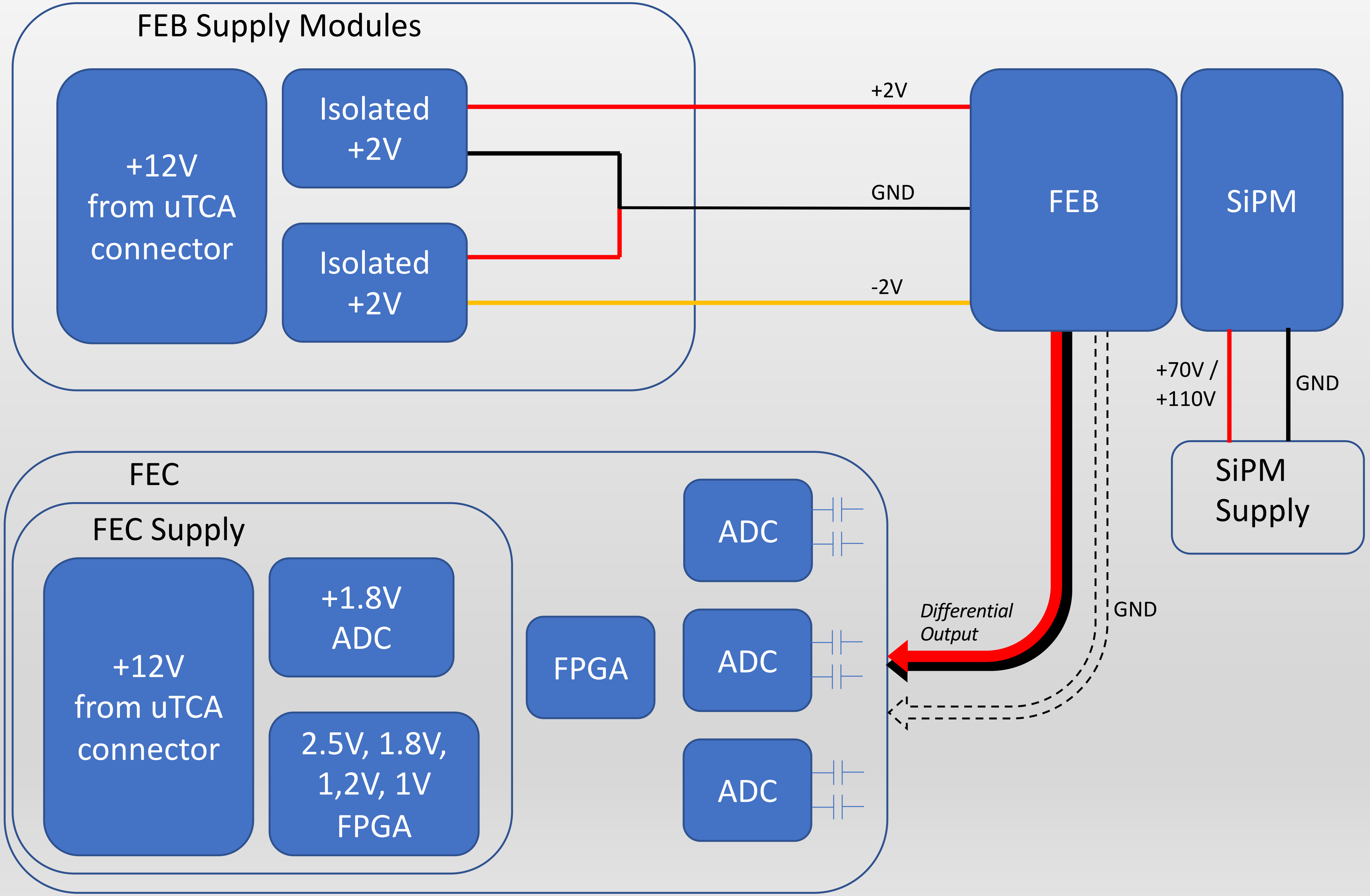
FEBs supply & connection

FEBs Low-Voltage supply on the row
High-Voltage power supply splitted for all 6 tiles



$I_{LV\text{-}BIAS} \sim 80mA \times \#_{FEB}$ @ -50°C

Power Supplies



Each tile delivered with its own calibration file, where V_{OP} all 16 SiPM are reported @ +25°C

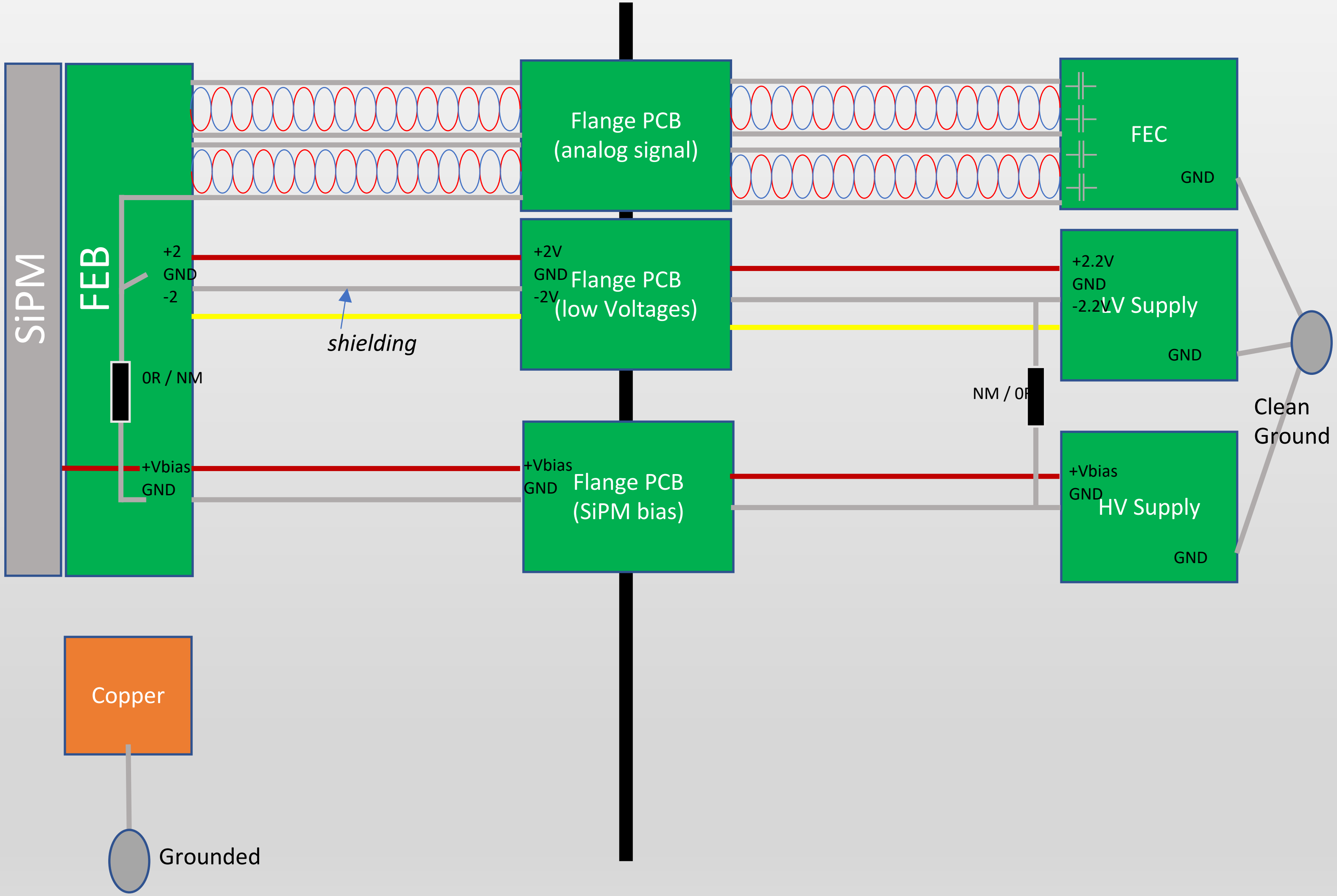
Temperature coefficient: +54 mV/°C

HV @ -50°C

$$\mathbf{V_{OP} - (0.054*75)}$$

HV must be doubled, due to the series connection carried out by the FEB

Grounding

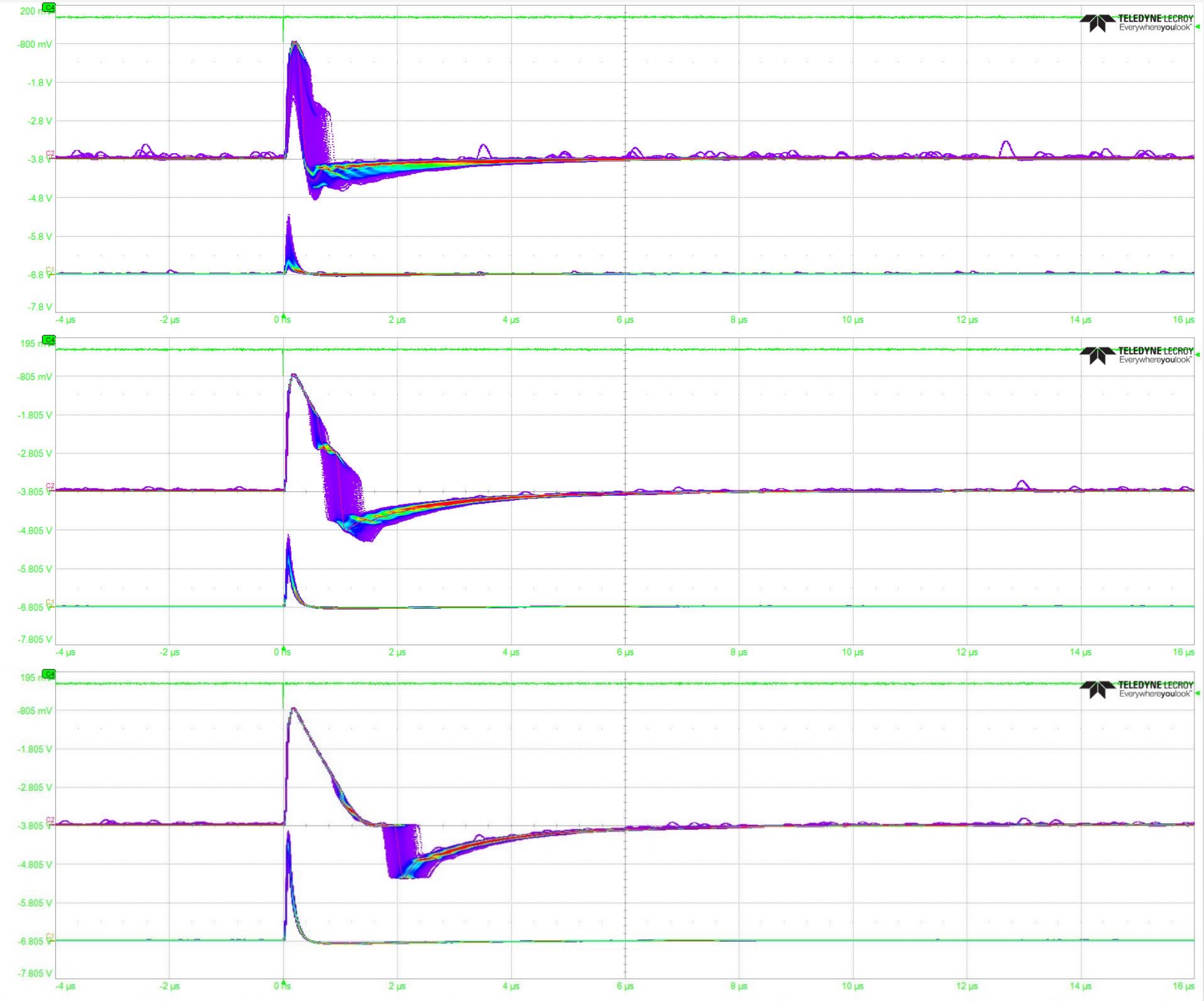


Different grounding schematics are feasible with the current hardware.

We are going to setup lab to study the different grounding connection.

The results of this study will be tested in the 1-to-1 prototype setup in IHEP.

Recovery Time



- We reduced the gain (1/20) of 1 FEB channel to have a «self calibration» of the light pulse.
- The «rebounce» happens after the TIA saturation.
- In the circled area the photon counting can be executed but it needs a careful evaluation of the baseline.

DCR MEASUREMENT

Dark Count Rate

Typ. 2000 / Max. 6000 (Typ. 13.9 / Max. 41.7)	cps/ch. (cps/mm²)

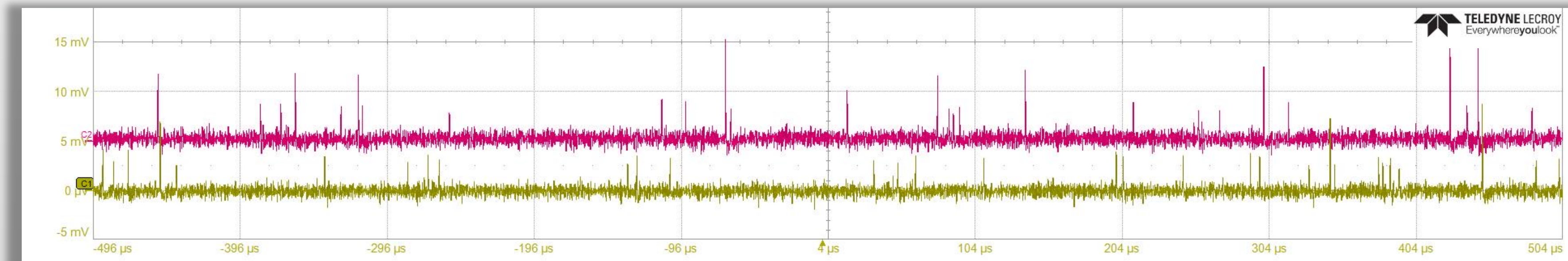
Count of events above a voltage threshold (halfway 0 and 1 pe) in 1 ms (averaged over 1k events, to simulate 1 second), normalized with overall area in a channel (12x12 mm² x8)

$$\mathbf{DCR} = (\overline{N_{1+}} * 1000)/1152 \quad [\text{Hz/mm}^2]$$

→ ~25 [Hz/mm²] @ +3 OV

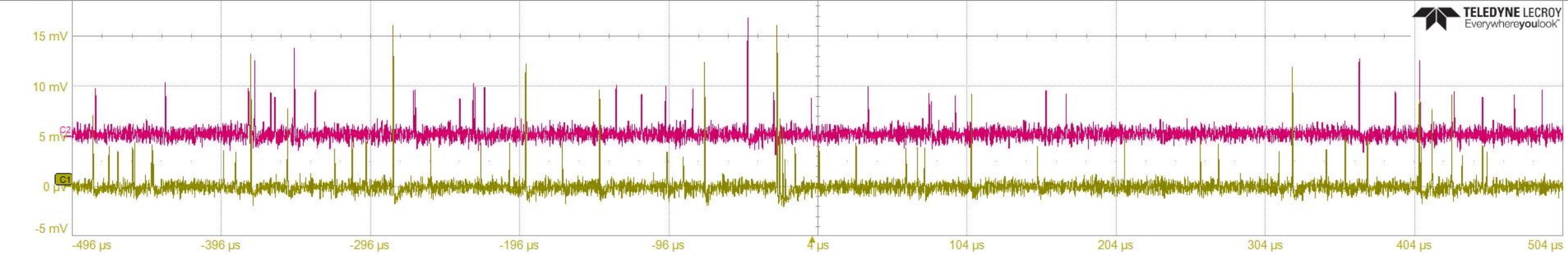
→ ~32 [Hz/mm²] @ +4 OV

+ 3V OV



Measure	P1:max(C1)	P2:max(C2)	P3:hsdev(F1)	P4:hsdev(F2)	P5:hmean(F1)	P6:hmean(F2)	P7:(P5/P3)	P8:(P6/P4)	P9:hmean(F1)	P10:hmean(F2)	P11:edge@lv(C1)	P12:edge@lv(C2)
value	1.17 mV	10.24 mV	> 157 µV	185 µV	> 3.51 mV	3.80 mV	> 22	21	> 1.07 mV	1.59 mV	32	28
mean	2.963 mV	3.528 mV	> 157 µV	185 µV	> 3.51 mV	3.80 mV	> 22	21	> 1.07 mV	1.59 mV	27.466	28.230
min	777 µV	1.18 mV	> 157 µV	185 µV	> 3.51 mV	3.80 mV	> 22	21	> 1.07 mV	1.59 mV	9	13
max	42.71 mV	26.27 mV	> 157 µV	185 µV	> 3.51 mV	3.80 mV	> 22	21	> 1.07 mV	1.59 mV	46	46
sdev	2.520 mV	2.318 mV	---	---	---	---	---	---	---	---	5.222	5.015
num	1.012e+3	1.012e+3	1	1	1	1	1	1	1	1	1.012e+3	1.012e+3

+ 4V OV



Measure	P1:max(C1)	P2:max(C2)	P3:hsdev(F1)	P4:hsdev(F2)	P5:hmean(F1)	P6:hmean(F2)	P7:(P5/P3)	P8:(P6/P4)	P9:hmean(F1)	P10:hmean(F2)	P11:edge@lv(C1)	P12:edge@lv(C2)
value	12.39 mV	11.75 mV	161 µV	181 µV	4.22 mV	4.56 mV	26	25	1.08 mV	1.57 mV	51	35
mean	4.883 mV	5.125 mV	161 µV	181 µV	4.22 mV	4.56 mV	26	25	1.08 mV	1.57 mV	37.249	36.817
min	721 µV	1.09 mV	161 µV	181 µV	4.22 mV	4.56 mV	26	25	1.08 mV	1.57 mV	17	17
max	30.23 mV	29.46 mV	161 µV	181 µV	4.22 mV	4.56 mV	26	25	1.08 mV	1.57 mV	59	60
sdev	4.051 mV	3.994 mV	---	---	---	---	---	---	---	---	5.986	6.104
num	1.008e+3	1.008e+3	1	1	1	1	1	1	1	1	1.008e+3	1.008e+3