A common readout unit for multichannel array detectors at HIRFL-CSR

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Abstract: The Cooling Storage Ring of the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR) is constructed to study nuclear physics, atomic physics, interdisciplinary science, and relative applications. A Common Readout Unit (CRU) has been designed for HIRFL-CSR to reduce the development time, production cost, and maintenance difficulties of the data transmission at HIRFL. With the Xilinx the Virtex 7 as its main FPGA, the CRU has 32 high-speed fiber optic interfaces to receive the data and two 10 Gigabit Ethernet links to transmit the data out. This paper will discuss the design and performance of the CRU.

Introduction

At present, the data transmission system in the particle experiment device is often constructed by the Versa Module Eurocard (VME) system and the PCI extensions for Instrumentation (PXI) system. The backplane of the VME chassis completes the connection between each backplane through the VME bus. Due to its parallel transmission, the transmission speed is limited to tens to hundreds of Mbps. The data transmission system designed based on PXI platform has the same disadvantages of low bandwidth, complex system, high cost and large size. With the rapid development of experiments in recent years, the particle energy has continued to increase, leading to a great increase in the number of particles produced by collisions, which has put forward higher requirements on the transmission capacity of the data transmission system, and the traditional bus of the data transmission system has been unable to solve this problem. To reduce the development time, production cost and maintenance difficulties of the readout electronics, a common readout unit (CRU) has been designed for generic control and data acquisition for multichannel array detectors at HIRLF-CSR. To meet the current and future speed requirements of the data transmission system, this article adopts optical fiber communication based on the Aurora 8B/10B protocol in the front-end, and utilizes a 10 Gigabit Ethernet interface based on TCP/IP in the back-end. The system is implemented using the Xilinx Virtex-7 series FPGA and complemented with peripheral circuit designs. The system is a small size, low cost and high transmission speed common readout unit (CRU).

The design of CRU

The CRU is composed of several functional modules: system clock and trigger interface, optical fiber array interface, gigabit Ethernet interface, 10 gigabit Ethernet interface , DDR3 interface, field programmable gate array (FPGA) (Xilinx virtex-7-485T) and its peripheral circuits . Through the system clock and trigger interface, the FPGA of CRU and detector system work at the same frequency and phase, and the CRU can receive the trigger signal from the detector trigger system. It can receive data collected from up to 32 FECs and transmit it to the CRU through a high-speed fiber array interface. The high-performance Xilinx virtex-7-485T (FFG1158) FPGA and DDR3 cache module with 75K Configurable Logic Blocks (CLBs) can complete the implementation of data processing algorithms and the reorganization of all channel data packets for the entire event. The 10 Gigabit Ethernet interface based on TCP/IP can transmit data to the data computer at high speed and stability. At the same time, control instructions and status feedback can be carried out on RCUs through Gigabit Ethernet.

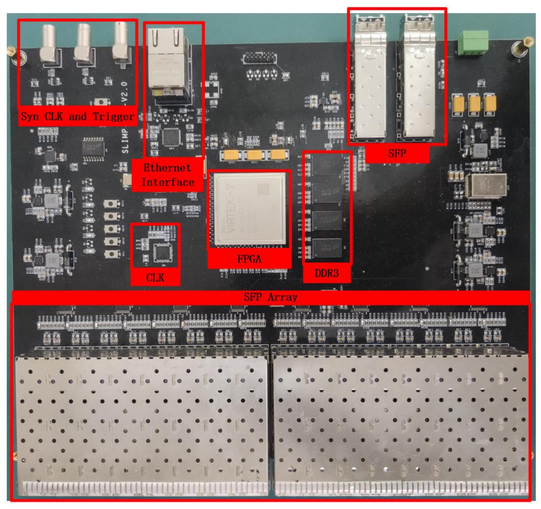

Figure 1. The picture of CRU

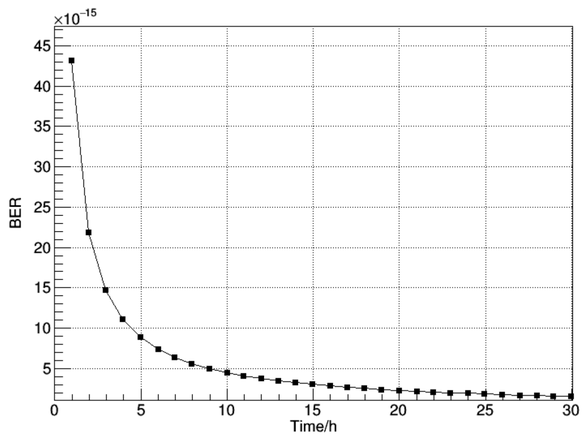

Figure 2. The result of BER test

Performance

To evaluate the functionality and performance of the CRU, we conducted a series of laboratory tests, including long-term stability hardware testing, communication link transmission performance testing, and joint testing with the Gamma detector system. Firstly, for electronic systems using fiber optic interfaces, long-term testing of eye charts and bit error rates can indicate hardware stability. The electric eye diagram has a large opening and clear outline, with an error rate of less than 2E-15. In order to verify the integrity of the communication link and the correctness of data communication within the FPGA, a FEC that can collect periodic sine signals has been added to the input. The collected data is transmitted to the data computer through fiber optic communication, DDR3, and 10 Gigabit Ethernet, and the collected data matches the input signal data. Finally, a CSI detector array unit was added and the detector system was tested using a 60Co radiation source. The test results clearly separated the full energy peaks of 1.17 and 1.33 MeV.

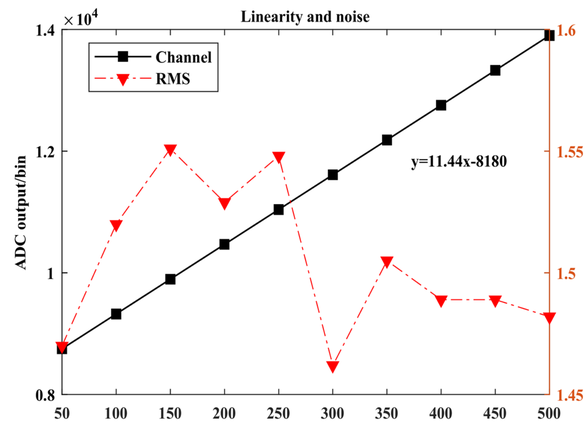

Figure 3. Linear and noise performance result

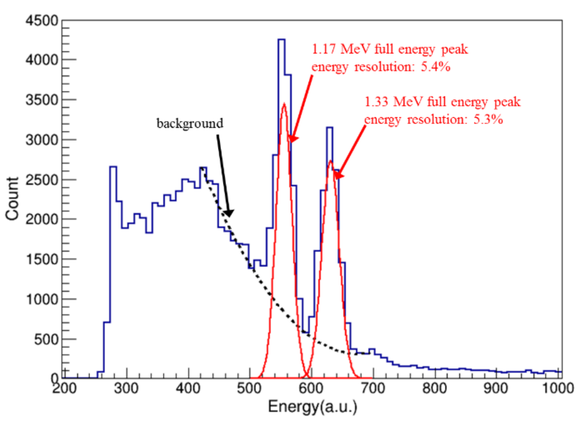

Figure 4. Measured Energy spectrum of the Co60

Conclusion

In this paper, a common readout unit (CRU) has been designed for generic control and data acquisition for multichannel array detectors at HIRLF-CSR. Using the proposed readout method, the data from the front-end cards (FECs) are sent to the CRU. The CRU aggregates data from FECs through 32 optical fiber interfaces. After packetizing and processing, the data is transmitted to the data computer through the backend 10 Gigabit Ethernet interface. Stability tests have been performed the CRU, no stop of readout or data error was seen on the optical fiber link and the 10 Gigabit Ethernet link.