Contribution ID: **180** Type: **Poster**

# A common readout unit for multichannel array detectors at HIRFL-CSR

*Thursday 5 October 2023 18:20 (20 minutes)*

The Cooling Storage Ring of the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR) is constructed to study nuclear physics, atomic physics, interdisciplinary science, and relative applications. A Common Readout Unit (CRU) has been designed for HIRFL-CSR to reduce the development time, production cost, and maintenance difficulties of the data transmission at HIRFL. With the Xilinx the Virtex 7 as its main FPGA, the CRU has 32 high-speed fiber optic interfaces to receive the data and two 10 Gigabit Ethernet links to transmit the data out. This paper will discuss the design and performance of the CRU.

## Summary (500 words)

1.Introduction

The Cooling Storage Ring of the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR) is constructed to study nuclear physics, atomic physics, interdisciplinary science, and related applications. The major experiments on the HIRFL-CSR are the Internal Target Facility (ITF), the External Target Facility (ETF) and the External-target Experiment (CEE). With the rapid development of experiments in recent years, high-performance detector readout electronics is essentail for the upgrade of the detectors. Hence, the CRU has 32 high-speed fiber optic interfaces to receive the data from the front-end electronics and two 10 Gigabit Ethernet links to transmit the data to the Data Acquisition System. In addition, the CRU also has a 1 Gigabit Ethernet interface, DDR3, and peripheral circuit design to complete the data transmission system. This paper will discuss the design and performance of the CRU.

2.The desgin of CRU

The CRU is composed of several functional modules: system clock and trigger interface, optical fiber array interface,gigabit Ethernet interface, 10 gigabit Ethernet interface, DDR3 interface, field programmable gate array (FPGA) (Xilinx virtex-7-485T) and its peripheral circuits . Through the system clock and trigger interface, the FPGA of CRU and detector system work at the same frequency and phase, and the CRU can receive the trigger signal from the detector trigger system. It can receive data collected from up to 32 FECs and transmit it to the CRU through a high-speed fiber array interface. The high-performance Xilinx virtex-7-485T (FFG1158) FPGA and DDR3 cache module with 75K Configurable Logic Blocks (CLBs) can complete the implementation of data processing algorithms and the reorganization of all channel data packets for the entire event. The 10 Gigabit Ethernet interface based on TCP/IP can transmit data to the data computer at high speed and stability. At the same time, control instructions and status feedback can be carried out on RCUs through Gigabit Ethernet.

3.Performance

To evaluate the functionality and performance of the CRU, we conducted a series of laboratory tests, including long-term stability hardware testing, communication link transmission performance testing, and joint testing with the Gamma detector system. Firstly, for electronic systems using fiber optic interfaces, long-term testing of eye charts and bit error rates can indicate hardware stability. The electric eye diagram has a large opening and clear outline, with an error rate of less than 2E-15. In order to verify the integrity of the communication link and the correctness of data communication within the FPGA, a FEC that can collect periodic sine signals has been added to the input. The collected data is transmitted to the data computer through fiber optic com-

munication, DDR3, and 10 Gigabit Ethernet, and the collected data matches the input signal data. Finally, a CSI detector array unit was added and the detector system was tested using a 60Co radiation source. The test results clearly separated the full energy peaks of 1.17 and 1.33 MeV.

**Authors:** LI, Xianqin (Institute of modern physics, Chinese Academy of Sciences); YANG, haibo; Prof. ZHAO, Chengxin (Institute of Modern Physics, CAS)

**Presenter:** LI, Xianqin (Institute of modern physics, Chinese Academy of Sciences)

**Session Classification:** Thursday posters session

**Track Classification:** Module, PCB and Component Design