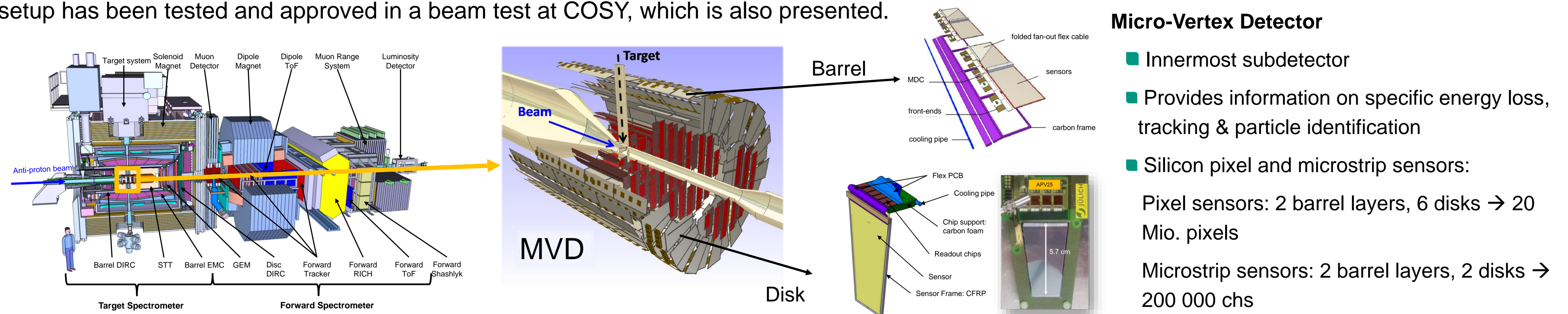


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PANDA (antiProton ANnihilation at DArmstadt) will be an experiment at the „Facility for Antiproton and Ion Research“. In this experiment proton-antiproton annihilation will be used to study the properties of the strong force. The PANDA detector will comprise of different sub-detectors for precise trajectory reconstruction, energy measurements and particle identification. In this contribution, the developed concept of the readout chain of the innermost subdetector, the Micro-Vertex Detector (MVD), is described. The realized readout chain for the MVD microstrip sensors is presented. The sensors and readout front-end have been integrated with the Module Data Concentrator (implemented on FPGA) to form the first fully functional detector module. This setup has been tested and approved in a beam test at COSY, which is also presented.

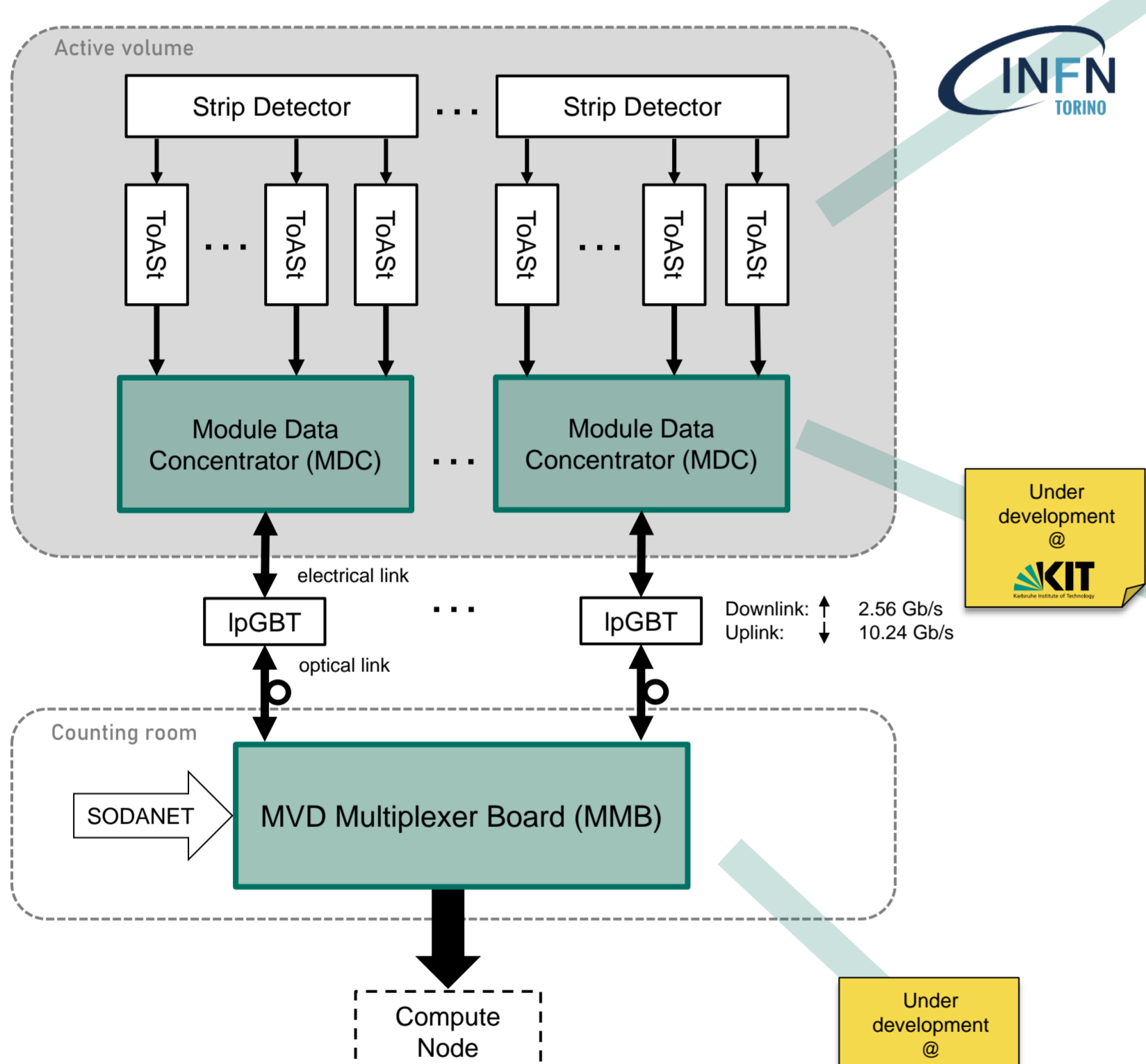


Micro-Vertex Detector

- Innermost subdetector
- Provides information on specific energy loss, tracking & particle identification
- Silicon pixel and microstrip sensors:
 - Pixel sensors: 2 barrel layers, 6 disks → 20 Mio. pixels
 - Microstrip sensors: 2 barrel layers, 2 disks → 200 000 chs

Microstrip Detector Readout Chain

- High granularity & expected occupancy → significant challenges in design of DAQ
- # 296 microstrip detector modules readout by IpGBT @ 10 Gb/s



MVD microstrip readout chain

MVD Multiplexer Board (MMB)

- AMC form factor, compatible with μ TCA & ATCA systems
- Each AMC card can manage up to 36 links @ 10 Gb/s (from/to detector)
- Readout based on ETH data link, 2x 100 GbE uplink to compute node
- Connection to Synchronization Of Data Acquisition (SODANET)
- AI algorithms for data processing, detector configuration & data quality monitor (DQM)
- Common and versatile DAQ system
- Standalone mode possible for testing

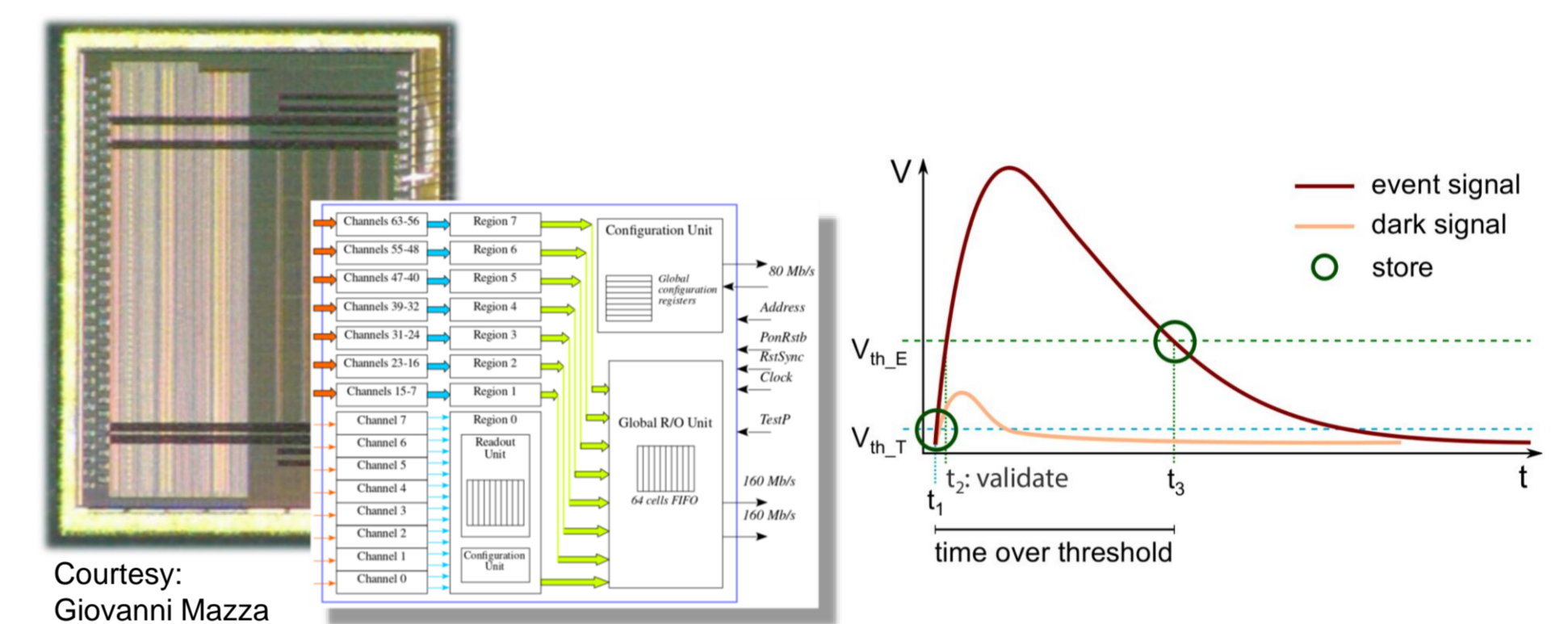
Front-end ASIC

- ToAST - Torino Amplifier for silicon Strip detectors
- UMC 110 nm CMOS technology
- 64 input channels
- Time of Arrival (ToA) & Time over Threshold (ToT) measurements
- Two output serial links @ 160 Mb/s
- Serial configuration protocol @ 80 Mb/s
- SEU protection via Triple Modular Redundancy

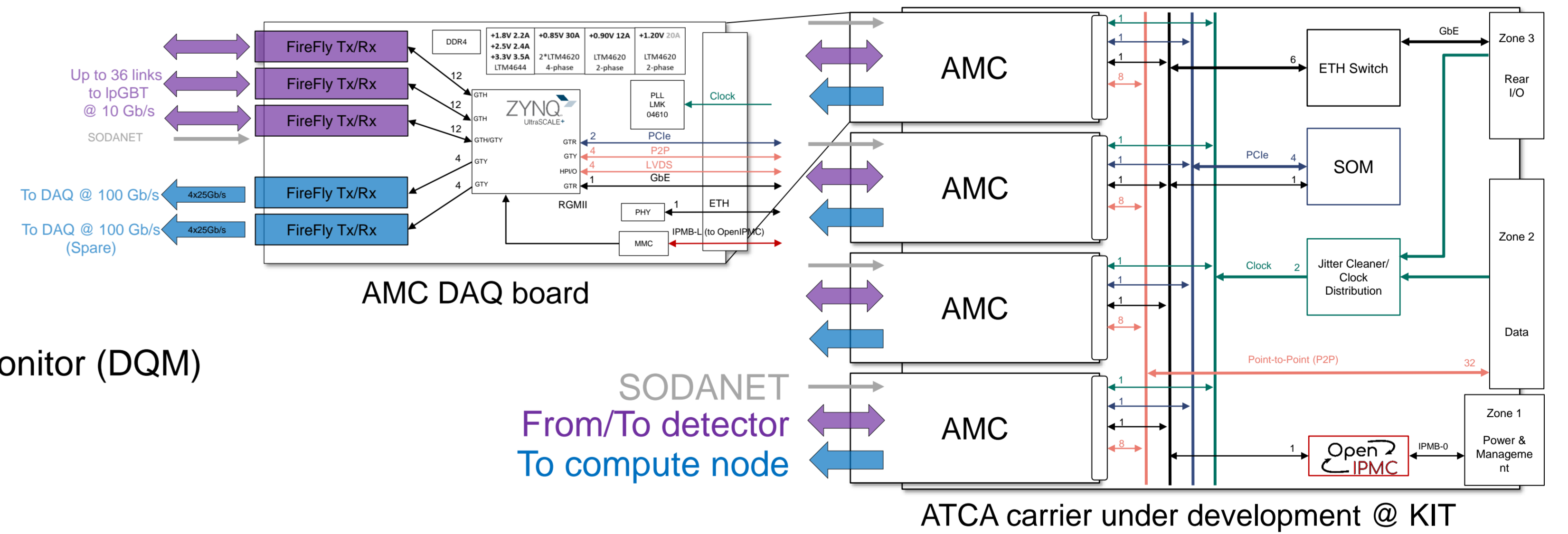
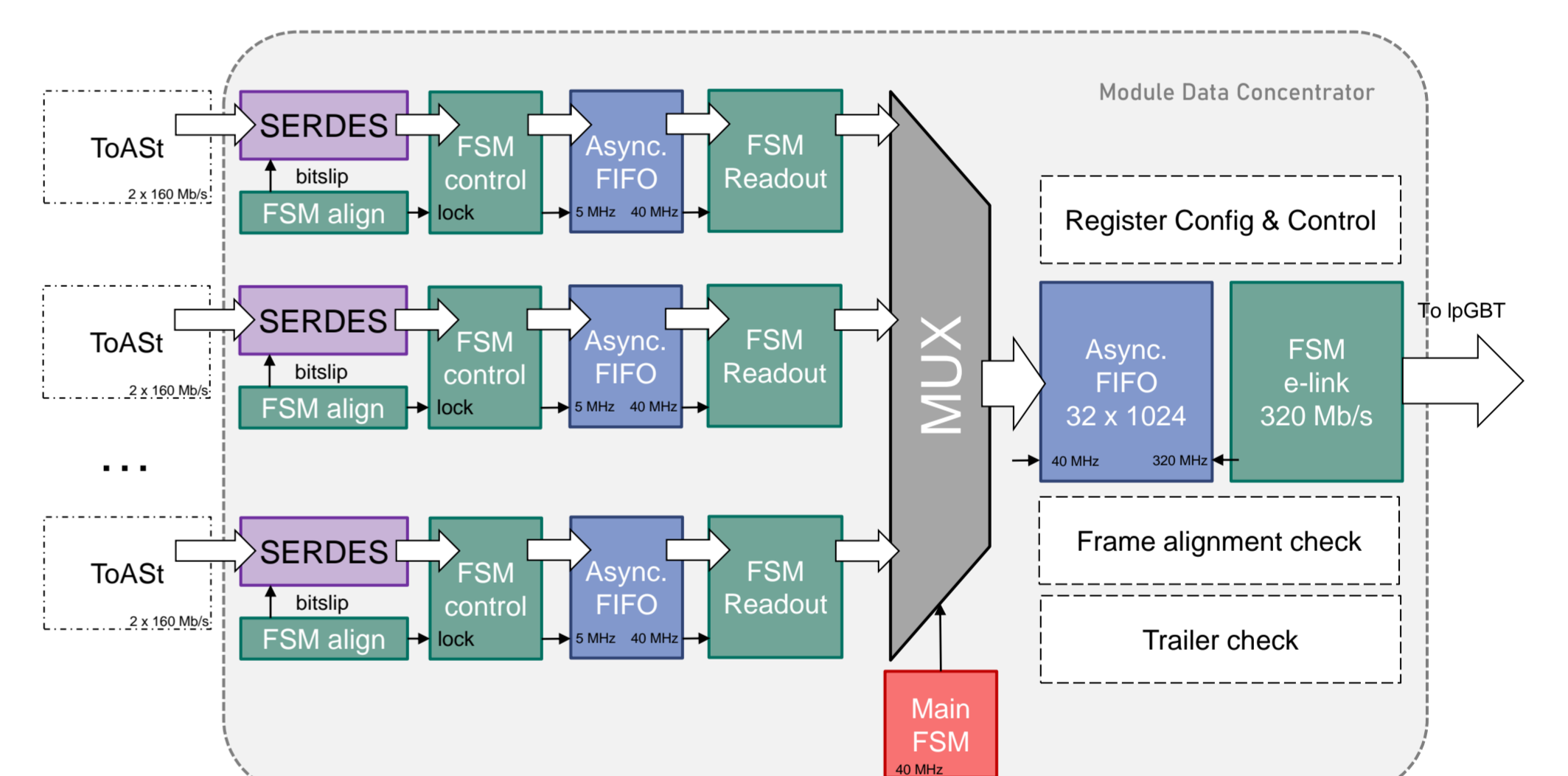
Module Data Concentrator (MDC) ASIC

- UMC 110 nm CMOS technology
- Zero-suppression
- Dynamic configuration of the high-speed links
- Intelligent multiplexing of up to 8 ToAST links
- Frame alignment logic
- Local detector configuration and slow control

Internal architecture of the ToAST ASIC

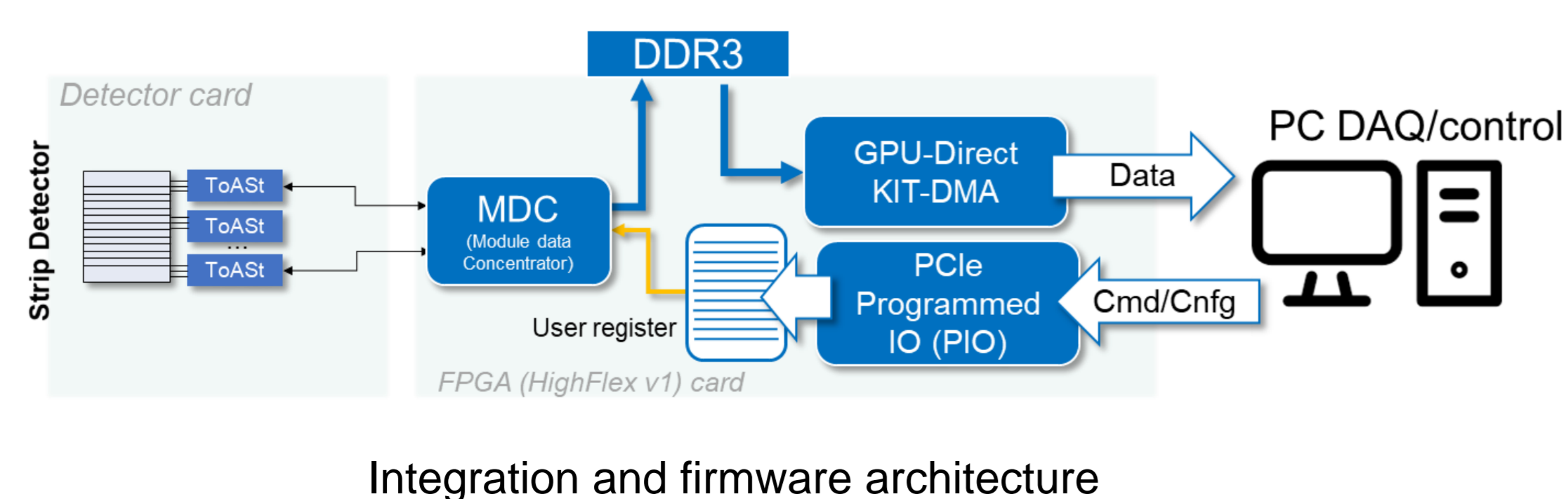


Internal architecture of the MDC ASIC

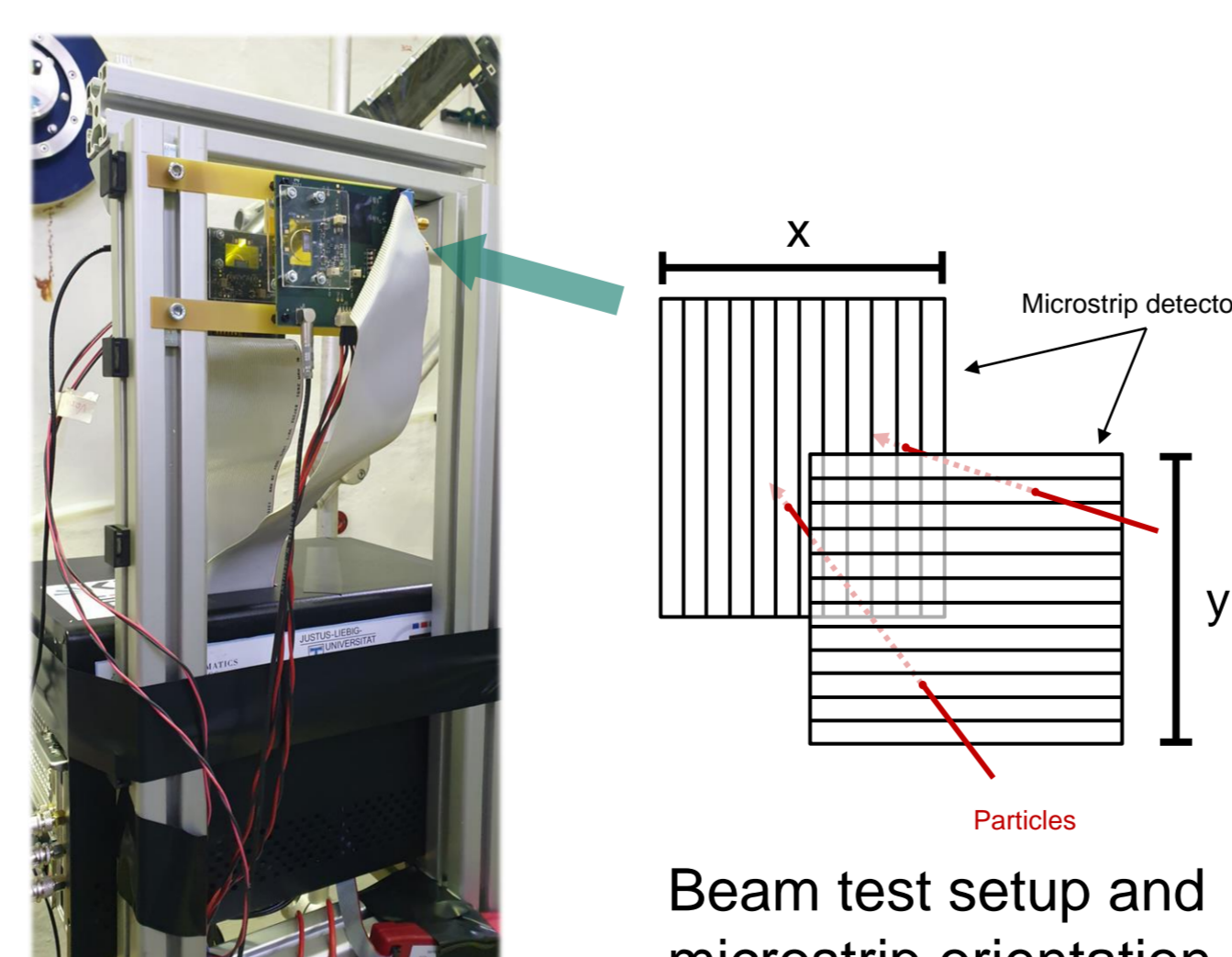
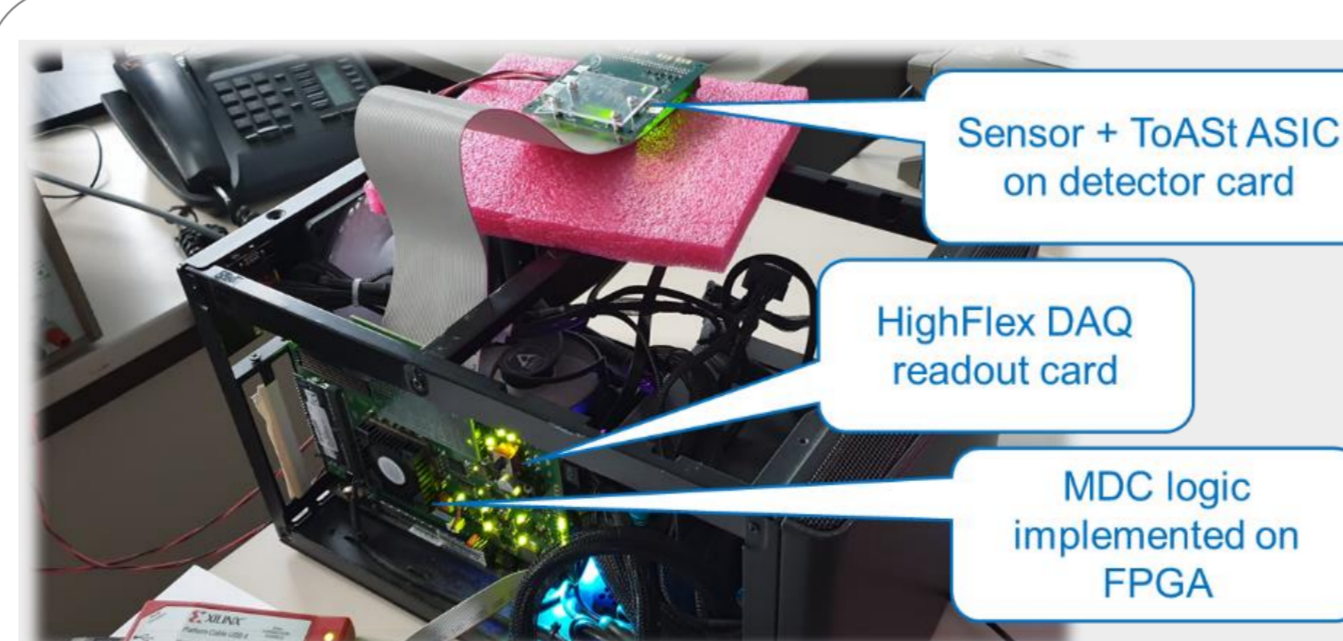


Integration of MDC with ToAST and sensor

- Commissioning of the setup @ KIT
- MDC-Implementation on FPGA
- Readout multiple ToAST → mimic detector module
- Readout based on FPGA-GPU-Direct communication
- Direct data transfer from FPGA to GPU memory → low latency
- Data throughput up to 120 Gb/s



Integration and firmware architecture



Beam Test Setup & Results

- Beam test @ COSY (Cooler Synchrotron, Jülich)
- Proton beam at different intensities
- Mechanical frame provided by Giessen University
- High-uniformity of the channels (very low threshold, gain dispersion)

