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## Data acquisition system of the PANDA Micro-Vertex Detector (MVD)

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The Micro Vertex Detector is a key component of the PANDA experiment at FAIR. This contribution focuses on the development of the Module Data Concentrator (MDC) ASIC for the configuration, time distribution and readout of the silicon microstrip subdetector system of the PANDA Micro-Vertex Detector (MVD). A first version of the MDC architecture has been developed on FPGA and integrated with the microstrip sensor and the front-end ASIC. The detector module has been integrated into the DAQ framework. The overall description of the MDC and the data acquisition system is presented and the first test results are discussed.

### Summary (500 words)

The PANDA (antiProton ANnihilation at DArmstadt) experiment will study the strong interaction in annihilation reactions between an antiproton beam and a stationary cluster jet target. The detector will comprise different sub-detectors for tracking, particle identification and calorimetry. The Micro-Vertex Detector (MVD) is the innermost part of the tracking system and is designed for precise tracking and detection of secondary vertices. It is equipped with silicon pixel and strip sensors and custom front-end electronics. For the readout of the double-sided silicon strip sensors, an ASIC called ToAST (Torino Asic for Strip readout) is being developed in 0.11  $\mu\text{m}$  CMOS technology by INFN Turin. The ASIC employs the Time-over-Threshold (ToT) technique for digitization and provides the Time of Arrival (ToA) of the crossing particle with a time resolution given by the clock frequency. To sustain the readout of the double-sided microstrip detector, a Module Data Concentrator (MDC) ASIC is under development at KIT. It will multiplex and process the data stream from the ToAST front-end and send it to back-end electronics, so called MVD Multiplexer Board (MMB). Up to 8 ToAST front-end chips of one detector module are controlled and read out by one MDC. The MMB board is under development at KIT, it will collect and process the data coming from several MDC chips and transfer the results via multiple optical links to the computing nodes for global event building. The second prototype of the ToAST ASIC with 64 active channels has been produced by UMC. This ToAST chip has been integrated with the FPGA implementation of the MDC to form the first fully functional detector module. Beam tests have been performed at COSY (Cooler Synchrotron) facility located at Jülich. This paper focuses on the design of MDC ASIC and MMB board, the integration with the ToAST and sensor and the first preliminary test results.

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