CMS ECAL Upgrade Front End card. Design and performance.

Abstract

Upgraded version of the CMS electromagnetic calorimeter (ECAL) Front-End (FE) card is designed to provide the lossless data streaming and reliable control and synchronization of the on-detector Very-Front-End (VFE) units.
The initial card design, validated in the beam tests in 2018-2019, was significantly modified to support the fast and reliable access to the VFE cards components for initialization, calibration and optimization of the data flow. Details of this updated design, performance of the final version of the card as well as the quality control and quality assurance plane for the mass production stage will be discussed.

Summary

The CMS ECAL detector readout unit is the Readout Tower: matrix of 5x5 calorimeter cells signals from which are digitized by five Very-Front-End cards, each serving five cells. One Front-End card collect data from five VFE cards and send via fast optical links off-detector to the Barrel Calorimeter Processor (BCP).
The calorimeter cell signal is digitized by the custom ASIC (CATIA) on the VFE board by 12-bit ADC at 160MHz sampling rate. The high sampling rate is required by the design time resolution. The data from one cell can be transmitted by one e-link at 1.28Gb/s rate thanks to the lossless data compression implemented by the custom data transmission and concentration ASIC (LiteDTU). 25 data e-links are handled by four CERN custom gigabit transceivers (lpGBT).
One of lpGBTs is working it transceiver mode (Master) to provide clock distribution and control functions, while three others – in transmitter only mode (Slaves).
Both data conversion ASICs, CATIA and LiteDTU are quiet fancy devices with multiple functions like special calibration and test regimes, data alignment etc. and require significant slow control resources for initialization, calibration, and control via custom I2C interfaces.
The limited slow control capacity of the Master lpGBT is not sufficient for 25 readout channels, hence slow control functions of Slave lpGBTs are also used. In addition, CERN custom GBT-SCA ASIC is used to extend the ADC and GPIO capabilities.
The initial design of the FE card with I2C control via Master-Slave I2C chain, although functioning well, was too slow for the ECAL application. That lead to the Readout Tower initialization time of more that 10 minutes.
The final design of the slow control chain includes the Master-Slave lpGBT communication via fast EC link and Master lpGBT – GBT-SCA communication via EC link simulation by up- and down- e-links.
Details of the FE card design and final performance evaluated via system test of the full ECAL readout chain: VFE-FE-BCP in the laboratory conditions at the beam tests will be presented.

The quality assurance (QA) and quality control (QC) of the FE cards during the mass production will be performed via several procedures:

- Short ageing of all produced cards in the Owen followed by the full functional test at the custom Test Stand

- Long ageing of randomly selected fraction of cards to the about full life cycle of the boards
- Irradiation in the hadron beam a small randomly selected set of cards followed by the full functional test

Details of the testing procedure and QA/QC procedures will be presented.