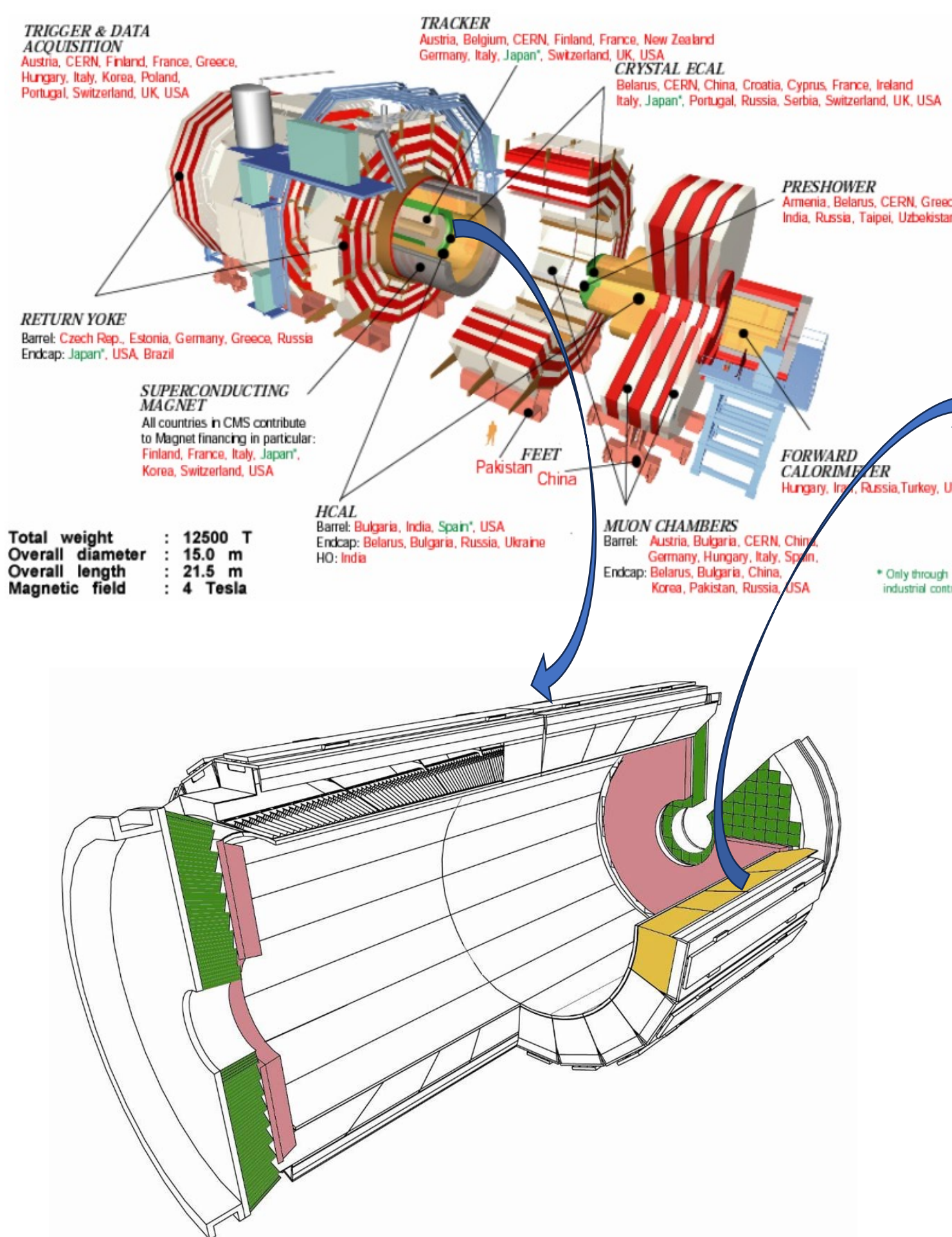
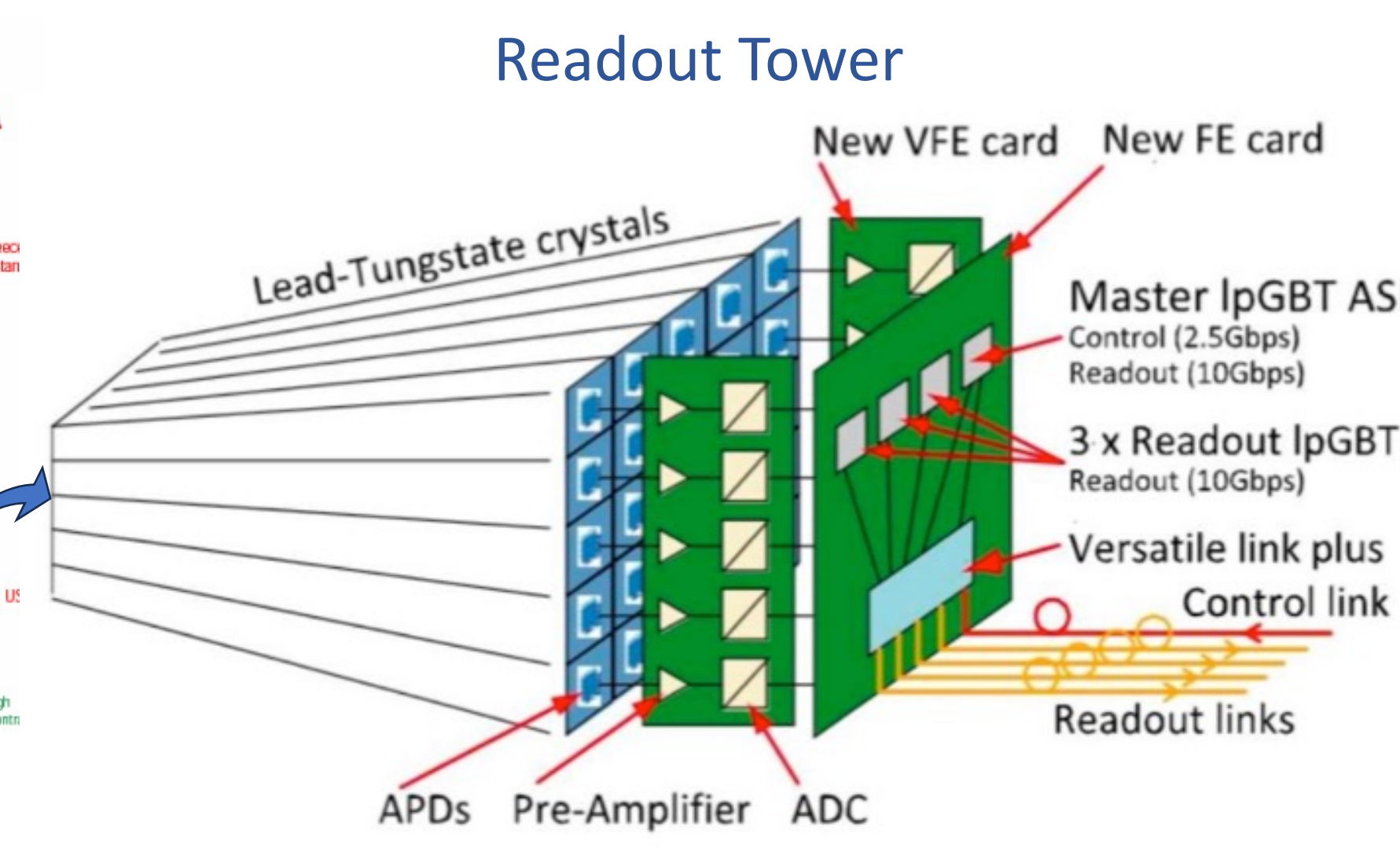


Phase II ECAL on-detector electronics Upgrade

Upgrade FE card functionality



Electromagnetic Calorimeter (ECAL)

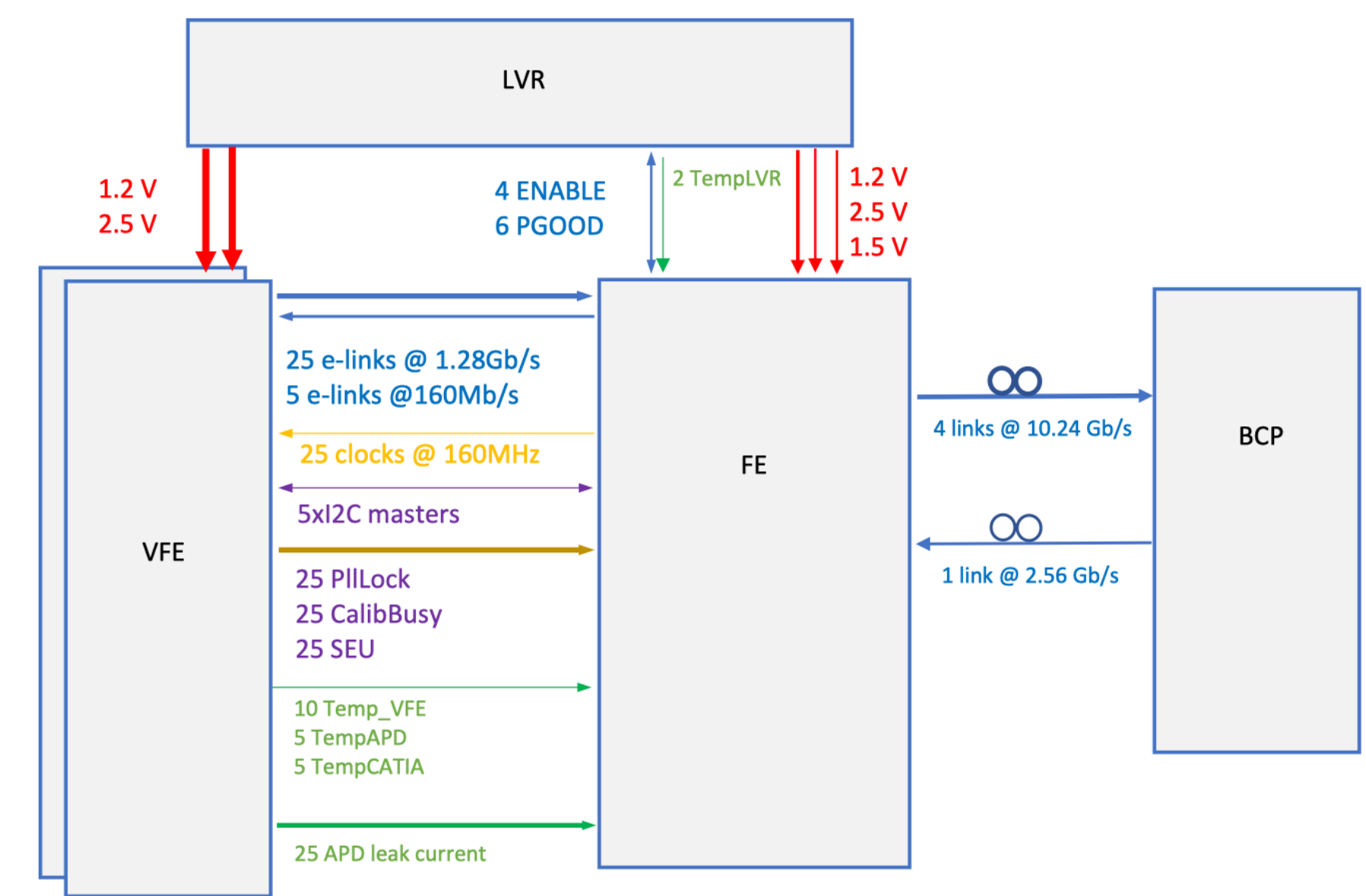


Readout unit of the CMS ECAL detector is the TOWER:

- 5x5 PWO crystals with scintillating light read out by 2xHAMAMATSU Avalanche Photo Diodes each
- 5x Very-Front-End (VFE) cards each containing 5 double gain pre-amplifiers (CATIA) and 5 ADC and data management chips (LiTE-DTU)
- 1x Front-End (FE) card with 4x IpGBT 1x GBT-SCA and 1x 4T1Rx optical transceiver
- 1x Low Voltage Regulator (LVR) card for VFE and FE powering

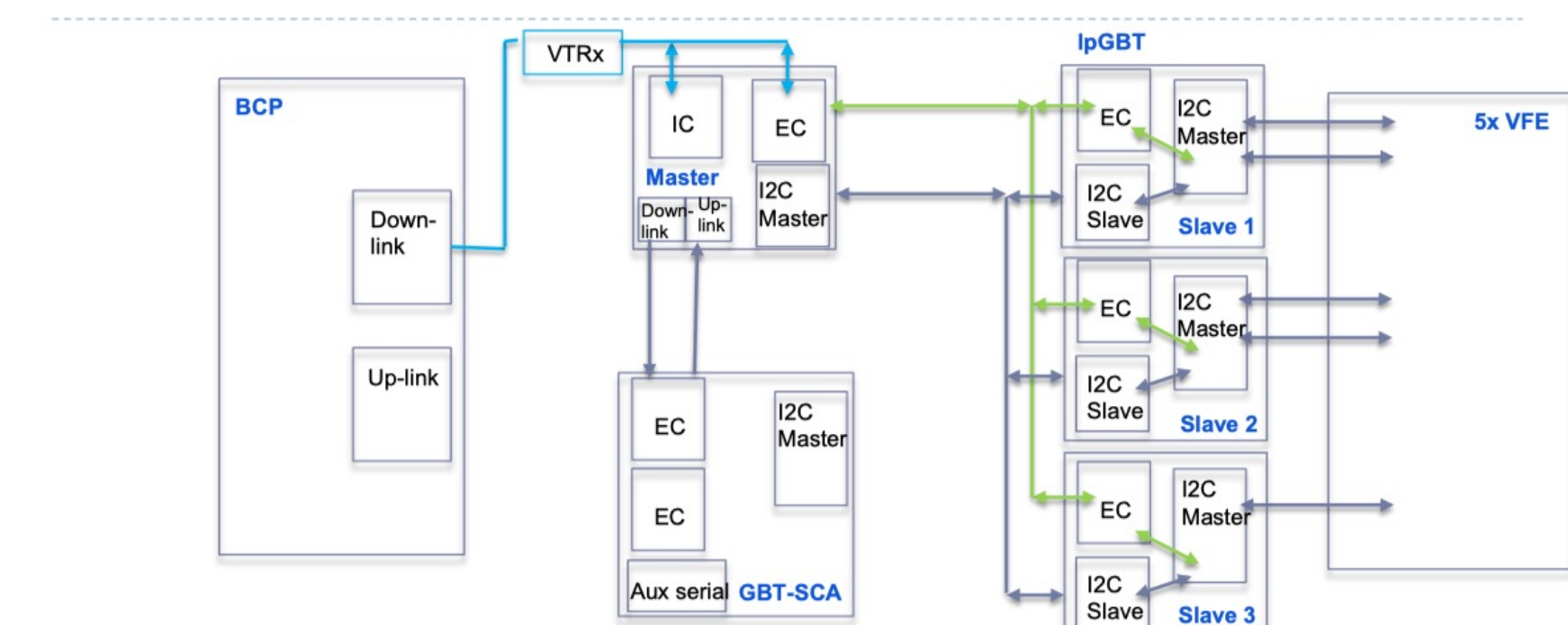
Upgrade FE card is the interface between intelligent VFE chips, CATIA and LiTE-DTU and powerful FPGA – based Barrel Calorimeter Processor (BCP). It provides:

- 160MHz clock distribution to the VFE readout channels
- VFE, LVR and FE chips configuration and control via I2C interfaces, one per VFE and LVR board
- Lossless data streaming from VFE readout channels via 1.28Gb/s serial links (IpGBT – links mechanism)
- Data transmission to BCP via four 10.24Gb/s optical links
- Chips status, temperature, power voltage, APD dark current readout via I2C interface and IpGBT optical up-link at 2.56Gb/s



Implementation

FE – VFE slow control

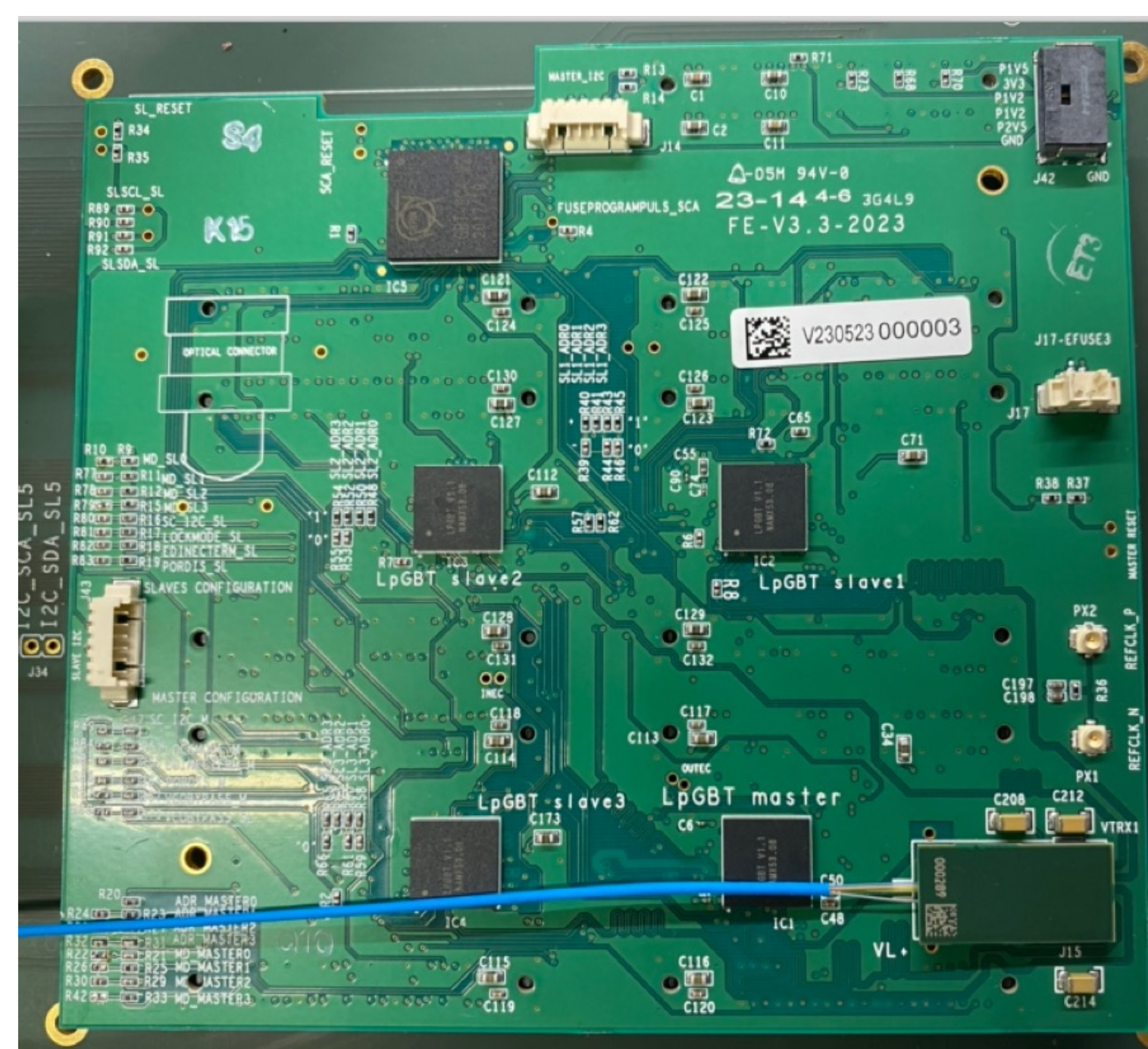


- GBT-SCA: EC link emulation by e-links
- IpGBT down-link: one link from special group, should run at 80MHz
- IpGBT up-link: one link from special group, Master will sample 80MHz data from SCA at 320MHz, BCP firmware have to deal with the repeating bits: 10 → 11110000
- Stable operation

FE PCB stack out

Layer	Material	Thickness	Notes
1	Prepreg	0.127 mm	
2	Dielectric	0.127 mm	
3	Prepreg	0.127 mm	
4	Dielectric	0.127 mm	
5	Prepreg	0.127 mm	
6	Dielectric	0.127 mm	
7	Prepreg	0.127 mm	
8	Dielectric	0.127 mm	
9	Prepreg	0.127 mm	
10	Dielectric	0.127 mm	
11	Prepreg	0.127 mm	
12	Dielectric	0.127 mm	
13	Prepreg	0.127 mm	
14	Dielectric	0.127 mm	
15	Prepreg	0.127 mm	
16	Dielectric	0.127 mm	
17	Prepreg	0.127 mm	
18	Dielectric	0.127 mm	
19	Prepreg	0.127 mm	
20	Dielectric	0.127 mm	
21	Prepreg	0.127 mm	
22	Dielectric	0.127 mm	
23	Prepreg	0.127 mm	
24	Dielectric	0.127 mm	
25	Prepreg	0.127 mm	
26	Dielectric	0.127 mm	
27	Prepreg	0.127 mm	
28	Dielectric	0.127 mm	
29	Prepreg	0.127 mm	
30	Dielectric	0.127 mm	
31	Prepreg	0.127 mm	
32	Dielectric	0.127 mm	
33	Prepreg	0.127 mm	
34	Dielectric	0.127 mm	
35	Prepreg	0.127 mm	
36	Dielectric	0.127 mm	
37	Prepreg	0.127 mm	
38	Dielectric	0.127 mm	
39	Prepreg	0.127 mm	
40	Dielectric	0.127 mm	
41	Prepreg	0.127 mm	
42	Dielectric	0.127 mm	
43	Prepreg	0.127 mm	
44	Dielectric	0.127 mm	
45	Prepreg	0.127 mm	
46	Dielectric	0.127 mm	
47	Prepreg	0.127 mm	
48	Dielectric	0.127 mm	
49	Prepreg	0.127 mm	
50	Dielectric	0.127 mm	
51	Prepreg	0.127 mm	
52	Dielectric	0.127 mm	
53	Prepreg	0.127 mm	
54	Dielectric	0.127 mm	
55	Prepreg	0.127 mm	
56	Dielectric	0.127 mm	
57	Prepreg	0.127 mm	
58	Dielectric	0.127 mm	
59	Prepreg	0.127 mm	
60	Dielectric	0.127 mm	
61	Prepreg	0.127 mm	
62	Dielectric	0.127 mm	
63	Prepreg	0.127 mm	
64	Dielectric	0.127 mm	
65	Prepreg	0.127 mm	
66	Dielectric	0.127 mm	
67	Prepreg	0.127 mm	
68	Dielectric	0.127 mm	
69	Prepreg	0.127 mm	
70	Dielectric	0.127 mm	
71	Prepreg	0.127 mm	
72	Dielectric	0.127 mm	
73	Prepreg	0.127 mm	
74	Dielectric	0.127 mm	
75	Prepreg	0.127 mm	
76	Dielectric	0.127 mm	
77	Prepreg	0.127 mm	
78	Dielectric	0.127 mm	
79	Prepreg	0.127 mm	
80	Dielectric	0.127 mm	
81	Prepreg	0.127 mm	
82	Dielectric	0.127 mm	
83	Prepreg	0.127 mm	
84	Dielectric	0.127 mm	
85	Prepreg	0.127 mm	
86	Dielectric	0.127 mm	
87	Prepreg	0.127 mm	
88	Dielectric	0.127 mm	
89	Prepreg	0.127 mm	
90	Dielectric	0.127 mm	
91	Prepreg	0.127 mm	
92	Dielectric	0.127 mm	
93	Prepreg	0.127 mm	
94	Dielectric	0.127 mm	
95	Prepreg	0.127 mm	
96	Dielectric	0.127 mm	
97	Prepreg	0.127 mm	
98	Dielectric	0.127 mm	
99	Prepreg	0.127 mm	
100	Dielectric	0.127 mm	

- 4x IpGBT chips, one in TRx mode (Master) and three in Tx mode (Slaves)
- 1x GBT-SCA chip for the APD dark current readout
- 1x 4T1Rx Versatile link optical transceiver



- Class 3 PCB
- 14 layers
- Micro-vias between layers 1-2, 2-3, 14-13, and 13-12
- Serial lines impedance control with 10% precision

Functionality tests

Stand-alone test

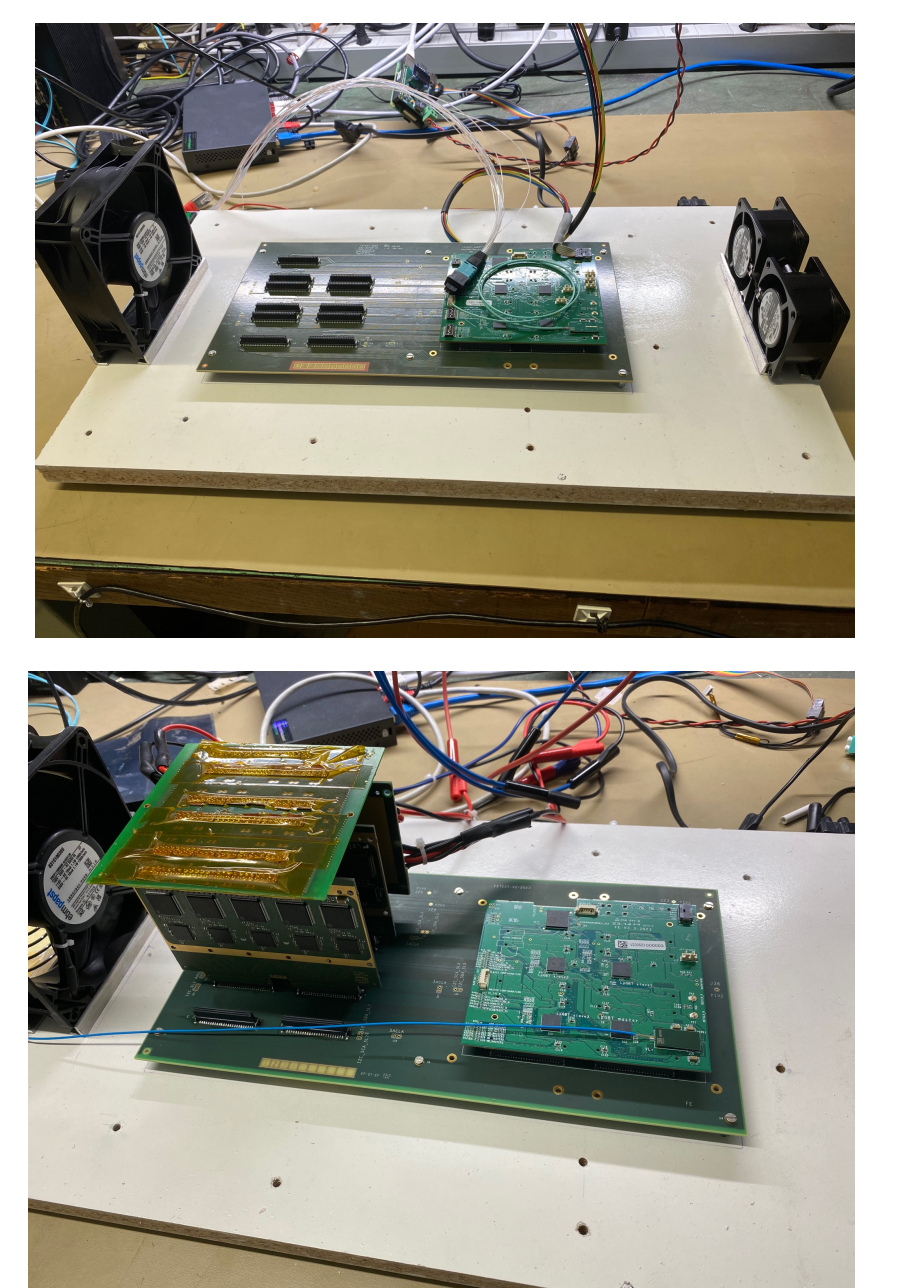
- Will be performed by the assembly company
- Electrical I2C control via PiGBT interface
- Electrical system clock from external clock generation
- IpGBT chips configuration
- I2C registers read/write

Functional test

- Will be performed at CERN upon reception
- Clock, control and readout via optical links from BCP
- Production LVR and VFE board for power, control and readout
- Full configuration of FE chips
- Full configuration of VFE chips
- Data alignment, PED and test pulse readout

Thermocycling and burning-in

- Climatic chamber
- Power to FE from external source
- Electrical I2C via PiGBT and Keithley switch
- Burning-in at 70C during 72 hours
- Periodic thermocycling 70C→9C→70C
- Periodic I2C initialization – configuration
- Full functional test at the end of operation

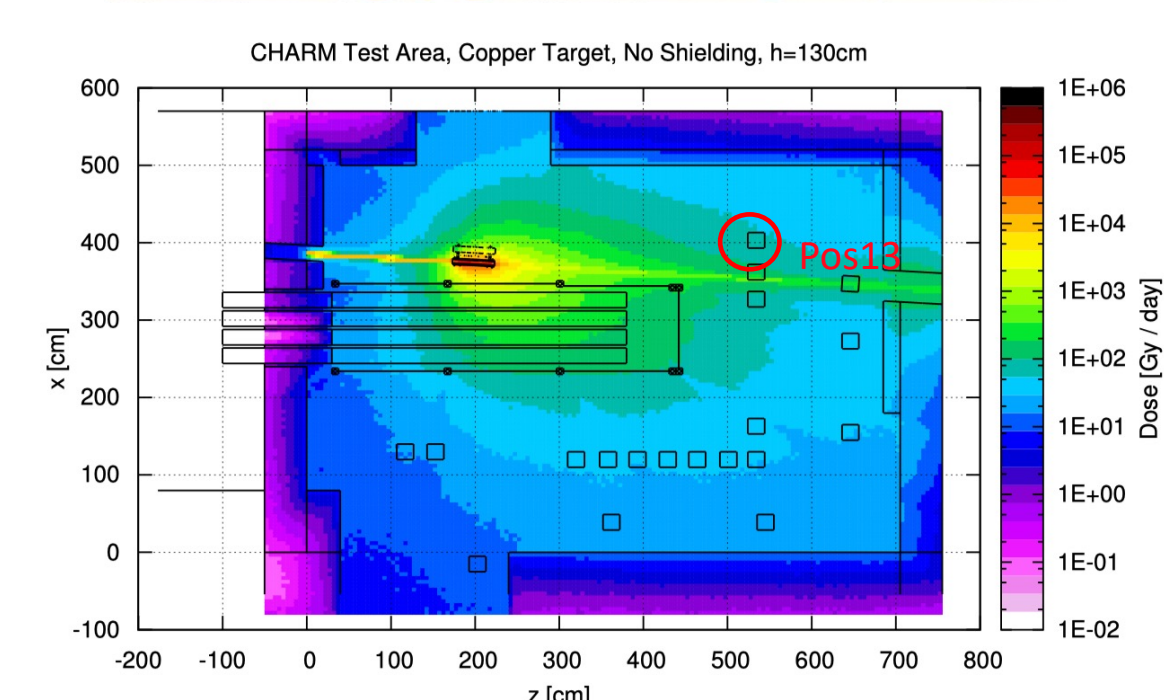


Special thanks to T. Gadek and C. Haller, ETH Zurich, for providing the VFE and LVR cards and for preparing the test setup for the readout tower test, respectively.

Full readout tower validation in radiation environment

- A complete tower with the latest versions of VFE and FE
- Five APD capsules connected to VFE_0
- Continues Reset/Config/Readout cycles by ECAL off-detector readout board (BCPv1)

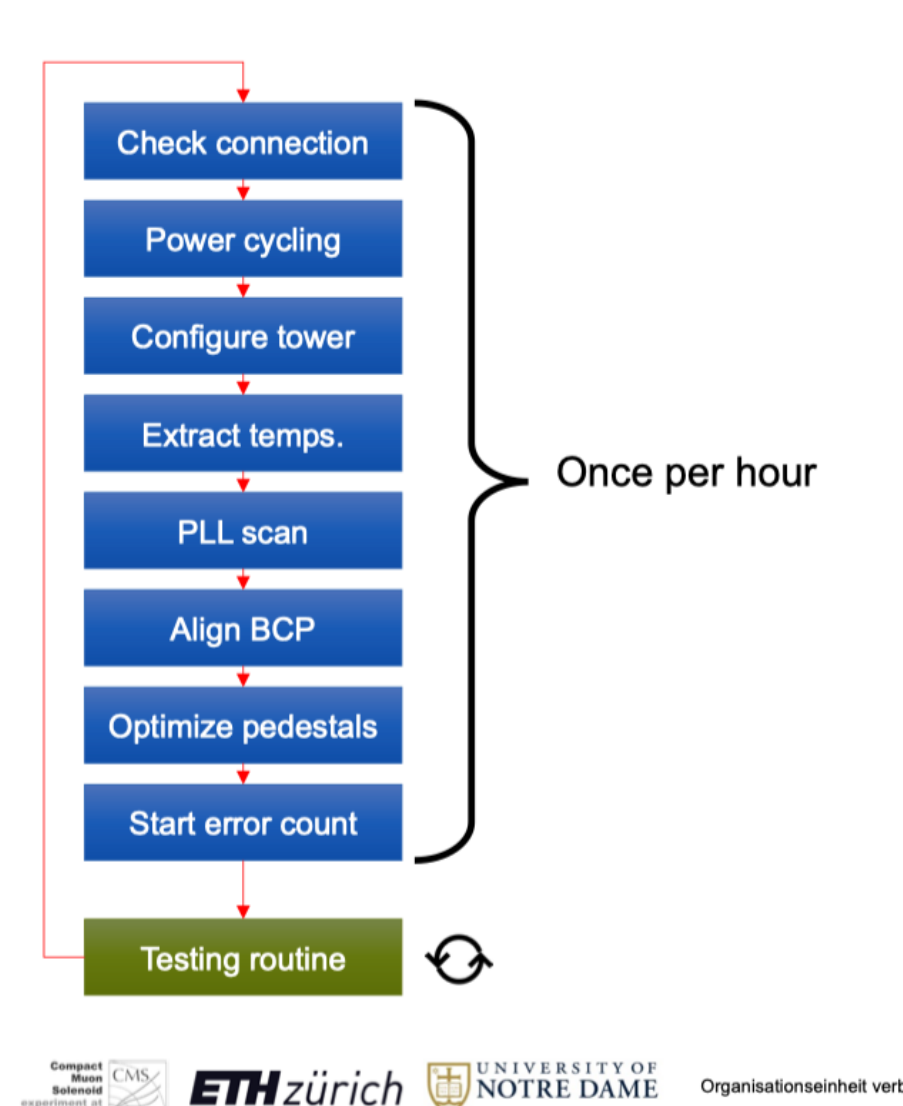
CERN CHARM facility



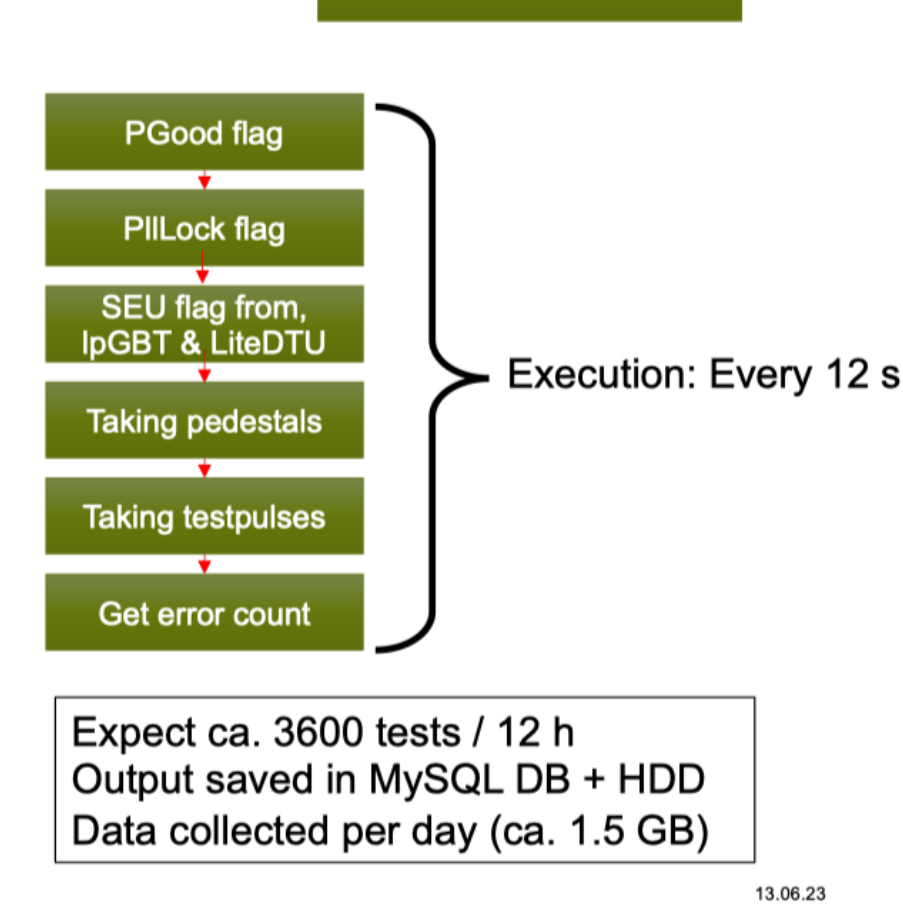
Tower at η=1.41 vs CHARM pos13

	HL-LHC (3000 fb ⁻¹)	CHARM (17 days)
Dose rate	9.57e-05 Gy s ⁻¹	7.84e-04 Gy s ⁻¹
Charged hadron flux	7.38e+04 cm ⁻² s ⁻¹	1.48e+06 cm ⁻² s ⁻¹
Total dose	5'740 Gy	1'380 Gy
Total Hadron fluence	4.43e+12 cm ⁻²	5.48e+12 cm ⁻²

Readout routine



Testing routine



- Stable operation in hostile radiation conditions (Charged hadrons flux 20 times higher than max. expected for ECAL tower at HL-LHC at η=1.41)
- SEU cases detected and handled by chips
- Good APD dark current readout by GBT-SCA ADC

