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# A Custom Discrete Amplifier-Shaper-Discriminator Circuit for the Drift Chambers of the R3B Experiment at GSI

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This contribution presents a pragmatic approach to read-out electronics for drift chambers used in particle physics experiments, specifically for the R3B experiment at GSI. The proposed circuit design uses discrete miniature SMD components and LVDS inputs of a low-cost FPGA to achieve a performance similar to the classic ASD8 ASIC. The presented approach offers an attractive solution for small to medium sized detector systems that require specialized read-out electronics but cannot afford the high cost and development effort associated with ASICs.

## Summary (500 words)

This contribution presents a pragmatic approach to read-out electronics for drift chambers used in particle physics experiments, specifically the R3B experiment at GSI.
The drift chambers used in this experiment and their 512 individual drift cells play a crucial role in particle tracking, momentum measurements as well as particle identification and require a specialized front-end electronics system to achieve the desired sensitivity and accuracy in terms of leading edge time (drift time) and pulse charge (particle energy loss). The aim was to develop discrete front-end electronics with similar performance as the classic ASD8 ASIC, which is no longer available due to its outdated manufacturing process.

The proposed circuit design consists of a discrete amplifier-shaper-discriminator circuit implemented in miniature SMD technology. Sixteen amplifier channels are integrated onto a single credit card-sized board which connects directly to the chamber. Each amplifier channel comprises three individual transistors in a TSLP-3 package (size of a 0402 resistor) and a number of 0201 passive components. The charge sensitive amplifier features a three-stage unipolar pulse shaper with a (measured) peaking time of $14\,ns$ and two pole-zero filters for ion tail suppression. The input impedance of the amplifier is $330\,\Omega$, which matches the impedance of the drift chamber cell. The overall gain of the circuit is $3.5\,mV/fC$.

Pulse discrimination for all 16 channels is carried out with the help of the numerous low-voltage differential signaling (LVDS) inputs of a low-cost FPGA.
The total power consumption of the ASD circuit is only $36\,mW$ per channel, while the transistor circuit alone accounts for $16\,mW$ per channel.

The front-end board feeds LVDS signals to an FPGA-based TDC data acquisition board which was also developed by our group. The employed TDC has a bin width of $416\,ps$, which yields a time measurement precision of $170\,ps$, and is thus sufficient for drift chambers.

A first test measurement was performed using a $^{55}Fe$ source with the chamber. The time-over-threshold spectrum shows clear peaks indicating the successful detection of the photo peak and the Argon escape peak at $6\,keV$ and $2.7\,keV$, respectively. The evaluation of the circuit's performance is ongoing, and further results will be presented at the time of the conference.

The presented approach demonstrates that modern SMD component dimensions and minimalist analog circuit design can be utilized to develop analog read-out solutions that can compete with ASIC solutions, at least in moderately high density detector set-ups. The proposed circuit design offers an attractive solution for

experiments that require specialized read-out electronics but cannot afford the high cost and development effort associated with ASICs.

**Author:** WIEBUSCH, Michael (GSI Helmholtzzentrum für Schwerionerforschung GmbH)

**Co-authors:** HEGGEN, Henning (GSI Helmholtzzentrum für Schwerionerforschung GmbH); HEIL, Michael (GSI Helmholtzzentrum für Schwerionerforschung GmbH)

**Presenter:** WIEBUSCH, Michael (GSI Helmholtzzentrum für Schwerionerforschung GmbH)

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