TWEPP 2023 Topical Workshop on Electronics for Particle Physics

The Prototype Design of PEB - a Component of the HGTD In-detector Electronics for the ATLAS Phase-II Upgrade

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Introduction to HGTD (High Granularity Timing Detector)

Silicon detector with coarse spatial resolution but precise timing for the ATLAS experiment
- ~3.6 million 1.3×1.3 mm^2 pixels with LGAD (Low-Gain Avalanche Detector) technology
  - 6.1 m^2 active area

- Pileup rejection
  - Time resolution at the start (end): 30 (50) ps per track / 35 (70) ps per hit
- Luminosity measurement
  - Count number of hits at 40 MHz (bunch-by-bunch)
  - Goal for HL-LHC: 1% luminosity uncertainty
- Two end-caps
  - z ≈ ±3.5 m from the nominal interaction point
  - 110 < r < 1000 mm
  - Active detector region: 2.4 < |η| < 4.0
- Each end-cap
  - Two instrumented disks, rotated by 15°
  - On each disk:
  - Double-sided layers mounted on a cooling plate
  - 3 ring layout for front-end modules

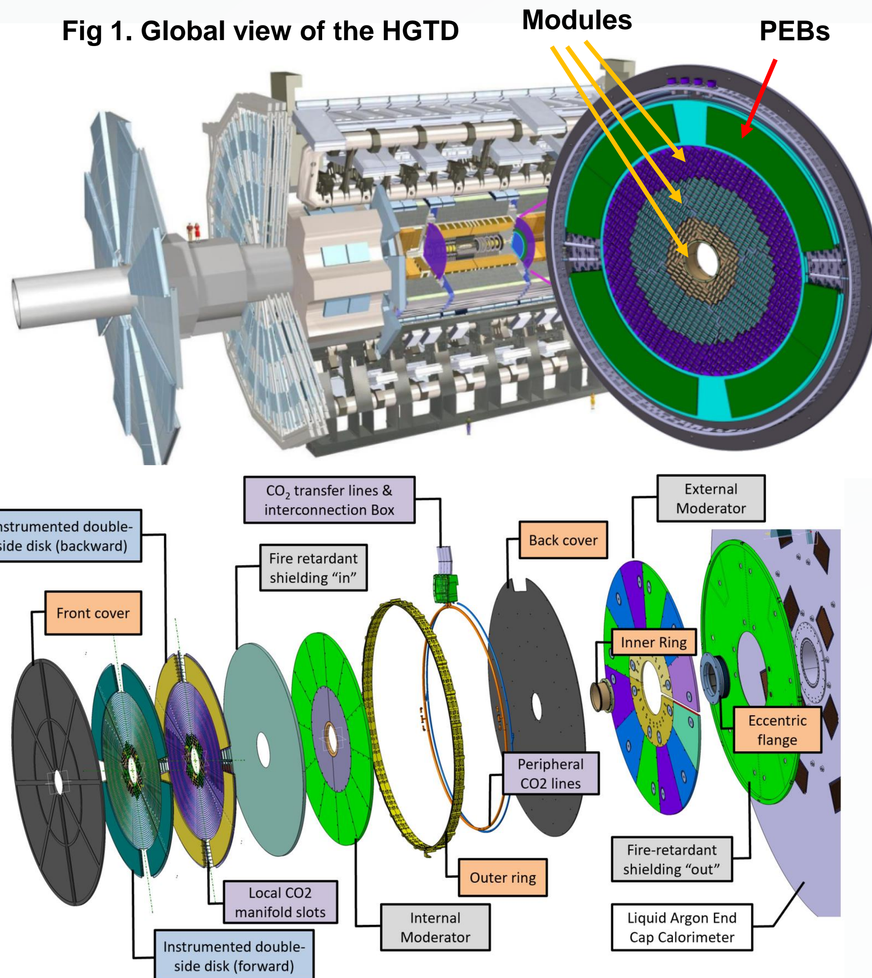


Fig 1. Global view of the HGTD

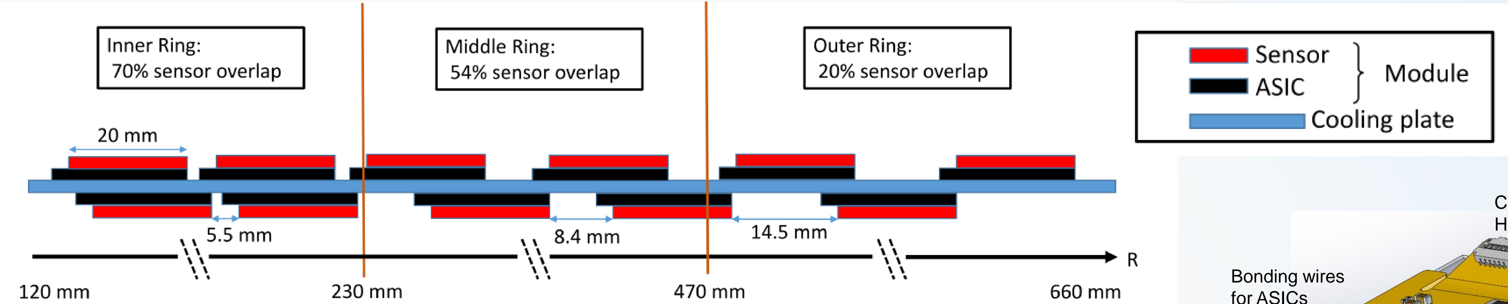


Fig 2. The schematic drawing shows the overlap between the modules on the front and back of a cooling disk. There is a sensor overlap of 20% for r > 470 mm, 54% for 230 mm < r < 470 mm and 70 % for r < 230 mm.

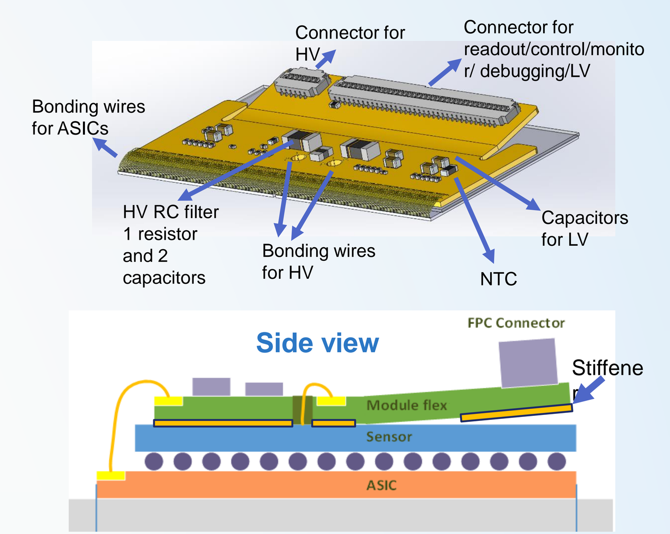


Fig 3. Front-end module

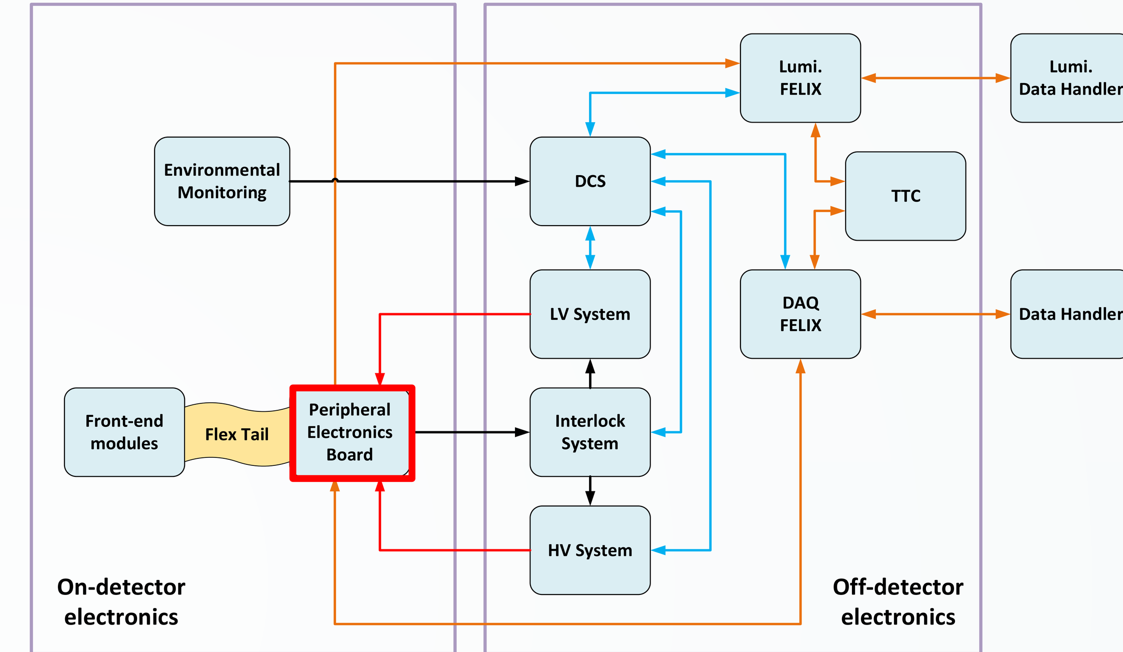


Fig 4. HGTD electronics architecture.

Basic functions of PEB
- Control, monitoring & data aggregation and transmission
- Power-supply distribution
  - Low voltage (LV) & High voltage (HV)
- Thermistor connection between the front-end modules and the interlock system

Peripheral Electronics Board (PEB)

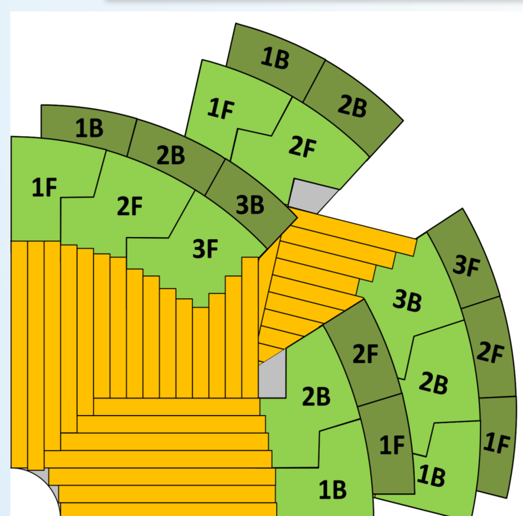


Fig 5. One quadrant of the two instrumented disks. The PEBs (in green) are attached to the readout rows

- Six types of PEB to be designed (front and back side) according to the installation location.
  - Board 1F, 2F, 1B and 2B can be used both on front and back
- The front-end modules are connected via flex tails, arranged in rows, to the PEB @ 660 < r < 920 mm

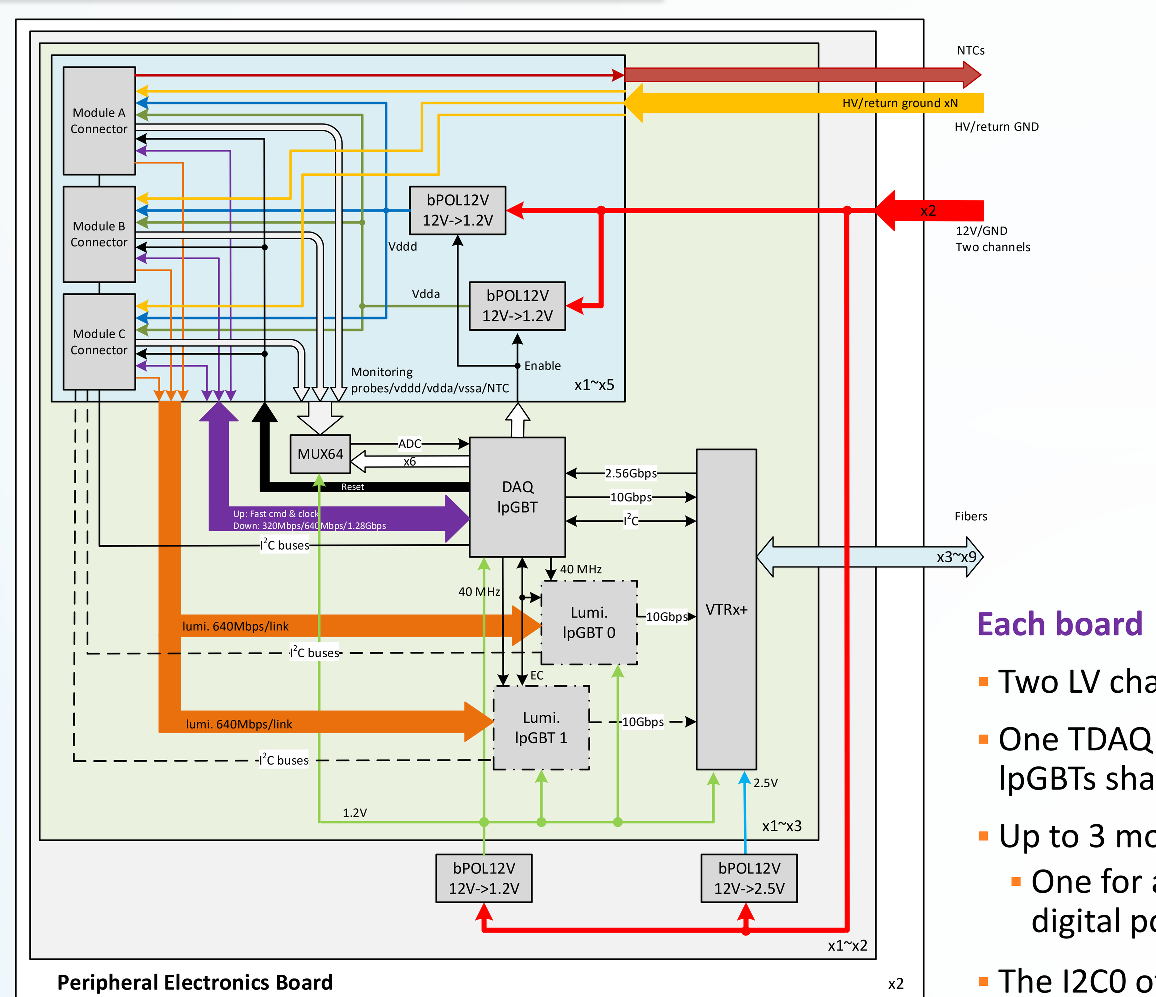


Fig 6. Conceptual design of the PEB

Tab 1. lpGBT elink assignments

Model ID	lpGBT Elinks	Mix230	Mix150	Mix310	Mix046(with lumi)	Mix00D(with 2 lumi)
M0	ECLK0, EDIN00, EDIN10, EDOUT00	1280, P0, I2C1	1280, P0, I2C1	1280, P0, I2C1	640, P0, I2C1	320, P0, I2C1
M1	ECLK1, EDIN01, EDIN11, EDOUT01	-	-	-	-	320, P0, I2C1, L640
M2	ECLK2, EDIN02, EDIN12, EDOUT02	-	-	-	640, P0, I2C1	320, P1, I2C2, L640
M3	ECLK3, EDIN03, EDIN13, EDOUT03	-	-	-	-	320, P1, I2C2, L640
M4	ECLK4, EDIN20, EDIN30, EDOUT10	1280, P0, I2C1	640, P0, I2C1	1280, P0, I2C1	640, P1, I2C2	320, P2, L_I2C0, L640
M5	ECLK5, EDIN21, EDIN31, EDOUT11	-	-	-	-	320, P2, L_I2C0, L640
M6	ECLK6, EDIN22, EDIN32, EDOUT12	-	640, P0, I2C1	-	640, P1, I2C2, L640	320, P2, L_I2C0, L640
M7	ECLK7, EDIN23, EDIN33, EDOUT13	-	-	-	-	320, P3, L_I2C1, L640
M8	ECLK8, EDIN40, EDIN50, EDOUT20	640, P1, I2C2	640, P1, I2C2	1280, P0, I2C1	320, P2, L_I2C1, L640	320, P3, L_I2C1, L640
M9	ECLK9, EDIN41, EDIN51, EDOUT21	-	-	-	320, P2, L_I2C1, L640	320, P3, L_I2C1, L640
M10	ECLK10, EDIN42, EDIN52, EDOUT22	640, P1, I2C2	640, P1, I2C2	-	320, P2, L_I2C1, L640	320, P4, L_I2C2, L640
M11	ECLK11, EDIN43, EDIN53, EDOUT23	-	-	-	320, P3 L_I2C2, L640	320, P4, L_I2C2, L640
M12	ECLK12, EDIN60, EDIN62, EDOUT30	640, P1, I2C2	640, P1, I2C2	640, P1, I2C2	320, P3 L_I2C2, L640	320, P4, L_I2C2, L640
M13	ECLK13, EDIN61, EDIN63, EDOUT31	-	-	-	320, P3 L_I2C2, L640	-

Each board
- Two LV channels
- One TDAQ lpGBT and 1~2 luminosity lpGBTs share one VTRx+
- Up to 3 modules share 2 bPOL12v
  - One for analog power, the other for digital power
- The I2C0 of TDAQ lpGBT is connected to the VTRx+ only

Basic patterns used in PEB, Mix XYZ
- X: number of module run 1.28 Gbps,
- Y: number of module run 640 Mbps,
- Z: number of module run 320 Mbps

Fig 7. Grounding scheme

Tab 2. Number of modules per PEB on the front and back sides.

PEB	Front side	Back side
1F	54 modules	55 modules
2F	52 modules	56 modules
3F	39 modules	-
3B	-	39 modules
2B	52 modules	48 modules
1B	54 modules	53 modules

PEB 1F prototype

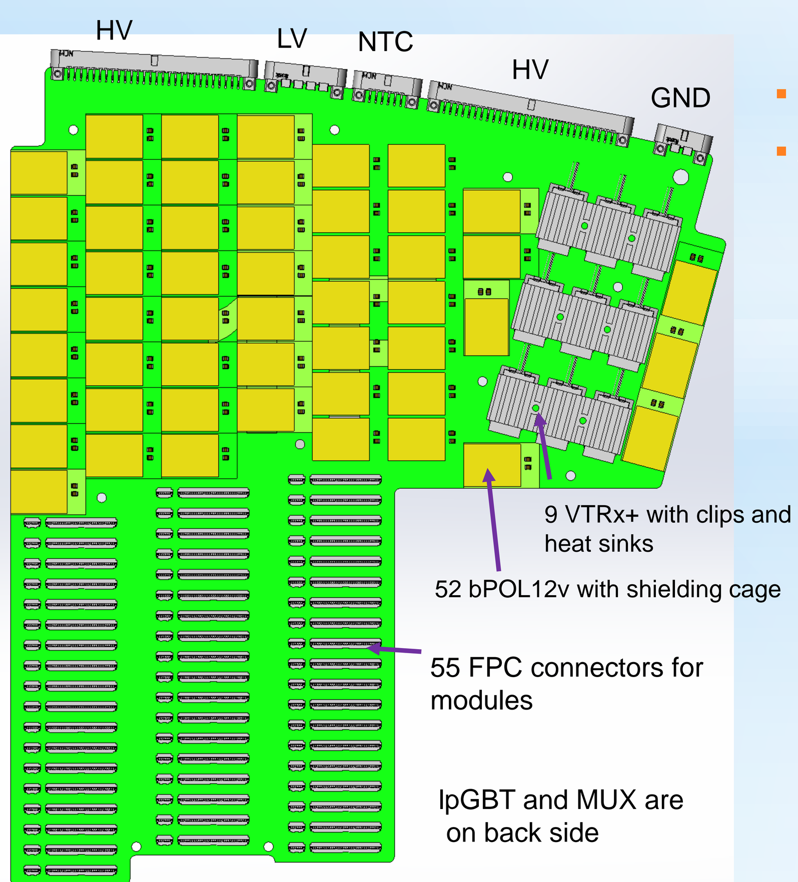


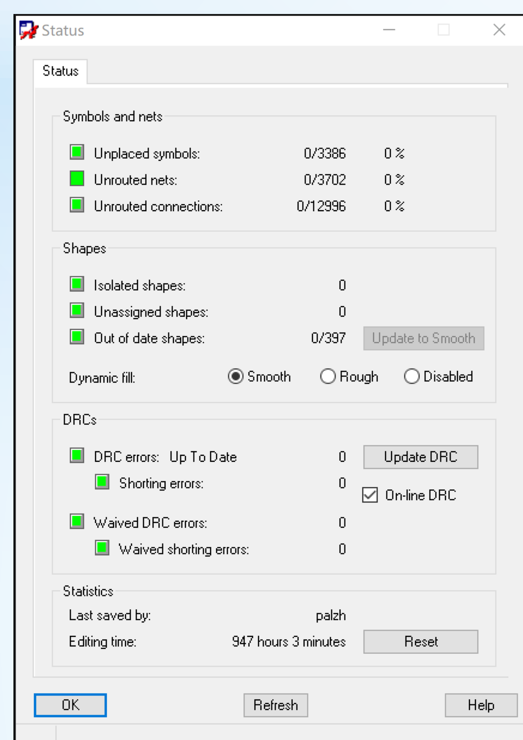
Fig 8. Top view of PEB 1F

Tab 3. Number of components in PEB 1F

Peripheral board	Modules	lpGBT	bPOL12v	MUX	VTRx+
1F	55	9+3	52	9	9

- PEB 1F, re-used on back side
  - 9 lpGBTs for timing
    - Front-end modules in 3 speeds according to occupancy
  - 3 lpGBTs for luminosity
    - 7 outermost modules in each row

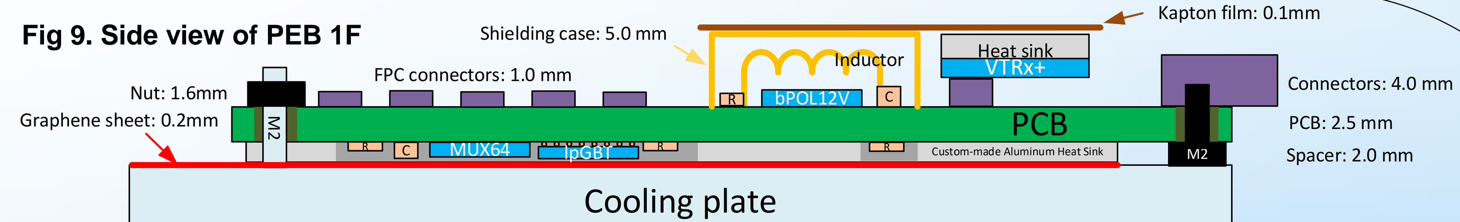
Complex PCB
- High speed, low loss multi-layer material
- Halogen free
  - EM-890 or IT-170/988 or R-5375(E)
- Impedance control
- 22 layers PCB for PEB 1F, includes:
  - 8 layers for signals
  - 2 layer for HV and HV return ground
  - 4 layers for ground
  - 8 layers for power



- HDI (High Density Interconnector)
  - Micro via
- VIPPO / POFV: Via-in-Pad Plated Over PCB

Physical Constraints
- Height < 10 mm
  - The space available for the electronics in the z-dimension is also very small: 9 mm with a 1 mm margin.

Fig 9. Side view of PEB 1F



Tab 4. Front-end module elink assignments in PEB 1F

Row ID	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21	F1/B21
Sequence ID	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
lpGBT ID	T6	T6	T3	T3	T6	T3	T3	T3	T0	T0	T0	T0	T0	T0	T0	T0	T0	T0
Model ID	M0	M4	M0	M4	M12	M8	M10	M12	M0	M2	M4	M6	M8	M9	M10	M11	M12	M13
Lumi ID	-	-	-	-	-	-	-	-	-	-	-	L0	L0	L0	L0	L0	L0	L0
Model ID	-	-	-	-	-	-	-	-	-	-	-	M0	M2	M4	M6	M8	M10	M12
Power Grp	C1	C1	C0	C0	C1	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0

Row ID	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20	F2/B20
Sequence ID	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
lpGBT ID	T7	T7	T6	T4	T4	T4	T4	T4	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1
Model ID	M0	M4	M8	M0	M4	M8	M10	M12	M0	M2	M4	M6	M8	M9	M10	M11	M12	M13
Lumi ID	-	-	-	-	-	-	-	-	-	-	-	L1	L1	L1	L1	L1	L1	L1
Model ID	-	-	-	-	-	-	-	-	-	-	-	M0	M2	M4	M6	M8	M10	M12
Power Grp	C3	C3	C1	C2	C2	C2	C2	C2	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1

Row ID	B19*	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19	F3/B19
Sequence ID	S19*	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
lpGBT ID	T8	T8	T8	T7	T5	T5	T5	T5	T5	T2	T2	T2	T2	T2	T2	T2	T2	T2	T2
Model ID	M0	M4	M8	M8	M0	M4	M8	M10	M12	M0	M2	M4	M6	M8	M9	M10	M11	M12	M13
Lumi ID	-	-	-	-	-	-	-	-	-	-	-	-	L2	L2	L2	L2	L2	L2	L2
Model ID	-	-	-	-	-	-	-	-	-	-	-	-	M0	M2	M4	M6	M8	M10	M12
Power Grp	C3	C3	C3	C3	C3	C3	C3	C3	C3	C2	C2	C2	C2	C2	C2	C2	C2	C2	C2