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The Prototype Design of PEB - a Component of the HGTD In-detector Electronics for the ATLAS Phase-II Upgrade

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The HGTD is a novel detector introduced to augment the new all-silicon Inner Tracker in the pseudo-rapidity range from 2.4 to 4.0, adding the capability to measure charged-particle trajectories in time as well as space. A prototype of Peripheral Electronics Board (PEB), which supports up to 55 front-end modules with 12 lpGBT, 9 VTRx+ and 52 bPOL12v, is developed to work as a bridge between the front-end modules and the off-detector TDAQ.
The on-going R&D effort carried out to study the readout and transmission chips, and the other components, supported by laboratory results, will also be presented.

Summary (500 words)

The increase of the particle flux (pile-up) at the HL-LHC with instantaneous luminosities up to ˜ 7.5 × 10ˆ34 cmˆ-2sˆ-1 will have a severe impact on the ATLAS detector reconstruction and trigger performance. The High Granularity Timing Detector (HGTD), an ATLAS Phase II upgrade project, will provide an accurate measurement of the time of the tracks (< 50 ps) in order to mitigate the effect of the pile-up in the object reconstruction as the jets, the electrons or the b-jets. In addition, the number of collected hits being proportional to the luminosity, it will provide an instantaneous measurement of the luminosity, which will be read out at 40 MHz.
HGTD is composed of 8032 front-end modules. Each module consists of two Low Gain Avalanche Detectors (LGADs) of approximately 2 × 2cmˆ2 bump-bonded to two ATLAS LGAD Timing Integrated Read-Out Chips (ALTIROC) and held together by a module flex (flexible PCB). These modules are arranged with overlap on the two sides on each disk. In order to facilitate the detector assembly, the modules will be mounted on support units forming detector units (a detector unit is a support unit with modules mounted on it). Each module will be connected to the Peripheral Electronic Boards (PEB) through a flex tail (another flexible PCB). The detector units and PEBs will be mounted on the HGTD cooling plates. The connections between on-detector and off-detector electronics are performed via optical fibers, high/low voltage cables, interlock cables and monitoring signal cables. The PEB acts as a bridge between the front-end modules and the off-detector systems. The optical fibers provide shared data streams for Timing, Trigger and Control (TTC), Detector Control System (DCS) and Data Acquisition System (DAQ), and dedicated data streams for the luminosity system.
For error-free data transmission at the bandwidths (320 Mbps, 640 Mbps, or 1.28 Gbps) required by the expected HGTD data volume, the PEB uses the low-power GigaBit Transmission chip (lpGBT) and the Versatile Link + Transceiver (VTRx+). The PEB also includes the 12 V to 1.2 V DC-DC converters (bPOL12v) for the digital and analogue voltages supplied to the front-end modules. The supply voltages are monitored using the internal multiplexed ADC on the lpGBTs. Since the input channel number of this ADC is limited to 8, a multiplexing chip is required to handle all the signals connected to PEB. A full custom 64-to-1 multiplexing ASIC (MUX64) has been developed with a radiation tolerance suitable for its implementation on the PEB.
According to the optimization of mirror structure for the layout of the modules, 6 types of PEBs need to be designed for HGTD. Based on previous development experience, the PEB 1F was chosen to be designed first as a prototype since it is the most complicated PEB type, which supports up to 55 front-end modules with 12 lpGBT, 9 VTRx+ and 52 bPOL12v in a very limited space. The requirements and overall specifications of the

electronics of HGTD will be presented as well as the technical design and the project status.

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