TWEPP 2023 TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS

A HIGH FREQUENCY RADIATION HARDENED DC/DC-CONVERTER WITH LOW VOLUME AIR CORE INDUCTOR

The hfrh-buck (high frequency radiation hardened-buck) is a radiation hardened DC/DC-converter operating at a high switching frequency of 100MHz with a small air core inductor of 22 nH. To ensure a high radiation dose, the circuit is designed with core transistors of a 65 nm TSMC technology. By stacking the transistors of the power stage, the converter can be supplied with a voltage of up to 4.8 V. Stable operation can be achieved at an output voltage of 1.2 V with a maximum load current of 1 A. The prototype demonstrates the ability to power parallel connected hybrid-pixel modules in the innermost layers.

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MOTIVATION

The readout electronics and voltage regulators of the pixel detectors are constantly being improved in order to function properly and meet the demands of increasingly harsh conditions. Detector systems must be as lightweight as possible, so it is advantageous to design the voltage regulators in the same technology as the detector readout chip to enable on-chip integration. The voltage regulators must operate reliably at high radiation doses, limited volume, long operating times and high magnetic fields. To meet these challenges, the development of innovative power supply concepts for use in high energy physics is of great interest.

Several approaches have been investigated in recent years, with a basic distinction being made between parallel and serial arrangements of hybrid pixel modules. For the upcoming Phase II SHLC upgrade, a serial power concept with a Shunt-LDO regulator has been selected as the baseline option for powering the pixel modules. Here, a DC/DC-converter based on a buck topology is presented that meets the requirements of the harsh environment and allows a conventional parallel supply scheme.

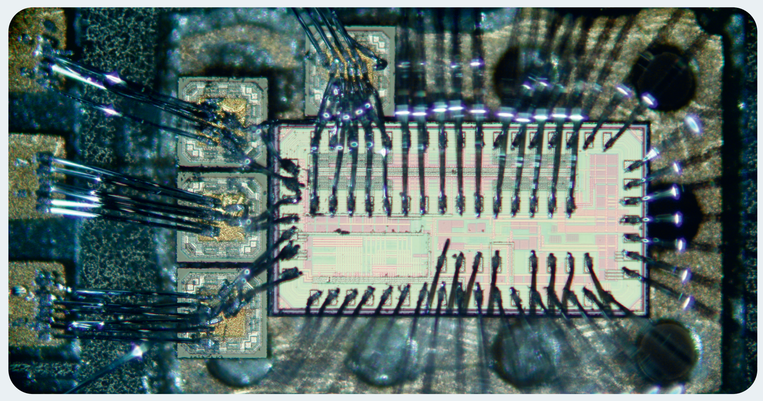
REQUIREMENTS

- A total **radiation dose of up to 1 Grad** has to be tolerated
  - → Whole circuitry built with **low voltage core devices** of a standard 65 nm TSMC technology (thin gate oxide) (voltage limit of core devices is 1.32 V)
- Thick gate oxide devices are required for high supply voltages
  - → **Stacked structures** are implemented to allow higher supply voltages by using core transistors
- Large transistors and fast switching edges lead to high voltage spikes at the switching instant and can cause faulty switching behavior and circuit failure
  - → Placing **large broadband silicon caps** close to the chip die improves decoupling and reduces the influence of parasitic effects
- **Limited space** and **high magnetic fields** require small air core inductors
  - → A **switching frequency of 100 MHz** was chosen to keep the inductor volume small

TESTCHIP

- The produced prototype has an area of 1 × 2 mm
- In the power paths, multiple bond wires are connected in parallel to keep parasitic effects low
- Bondable silicon caps (Murata) with ultra-large bandwidth have been placed in close proximity to the chip for optimal decoupling

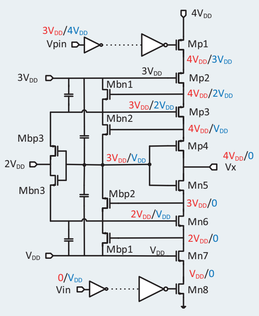
Supply Voltage	4.8 V
Output Voltage	1.2 V
Switching Frequency	100 MHz
Max. Load current	1 A
Indcutor & Capacitor	22 nH / 100 nF
Peak efficiency @ 400 mA	70 %
Technology	TSMC 65 nm (core devices) Max. voltage rating: 1.32V



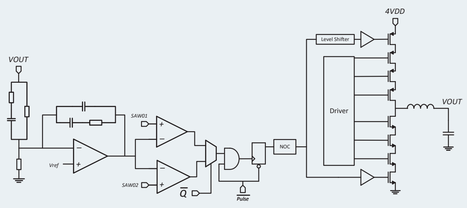
DESIGN OVERVIEW

Power Stage

- Switching stage built with 4 NMOS and 4 PMOS devices [2]
  - → Circuit switches between High state (red) and Low state (blue)
  - → Control signals of Mp1 and Mn8 determine the state of the circuit
- Biasing network [1] ensures safe operation of stacked transistors
  - → Biasing network monitors drain potential of cascode devices and applies the required gate voltage
  - → Ensures that cascode devices remain within their voltage limits
- The signal for the upper PMOS (Mp1) device is raised by a capacitive floating level shifter



PWM REGULATION



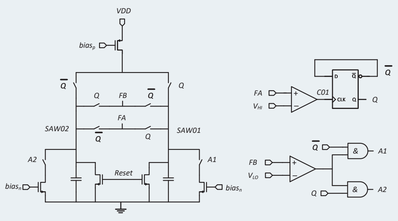
System Overview

- A PWM voltage mode control with type 3 (PID) compensation is selected to control the output voltage
- The digital logic becomes active and closes the PMOS stage as soon as a new switching cycle begins
- This reduces the risk of faulty switching due to noise on the comparator inputs

Sawtooth Generator

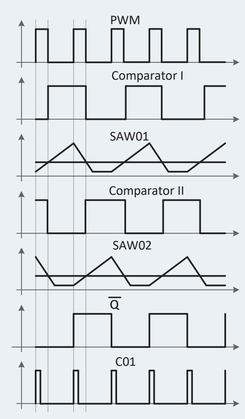
- Concept based on two 180° phase-shifted triangular waveforms to ensure fast switching times with small duty cycles [3]
- Two capacitors are alternately charged and discharged by a constant current (fast falling edges can be avoided)
- An upper and lower threshold voltage is defined to ensure that the biasing devices remain in saturation

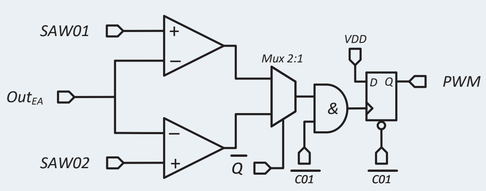
$$V_{HI} = V_{DD} - V_{DSAT} \;\&\; V_{LO} = V_{DSAT}$$



PWM Generation

- The PWM process is based on an approach where 2 comparators are activated on the rising edge of the corresponding sawtooth signal
- The sawtooth signals are phase-shifted by one switching cycle
- During the rising phase of one of the sawtooth voltages, the corresponding comparator output is selected to define the PWM control signal by means of a multiplexer. At the same time, the second sawtooth voltage is slowly falling as the corresponding capacitor in the oscillator discharges. The multiplexer toggles between the two comparators in each switching period.

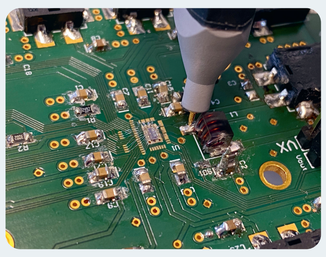




MEASUREMENTS

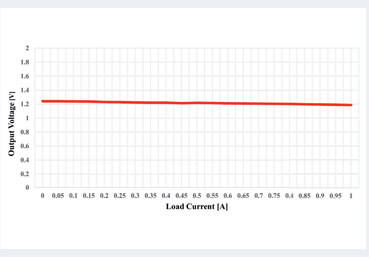
Transient Measurement

- The testchip shows a stable performance over the entire load range up to 1 A
- Measurements at sensitive voltage nodes were performed with an active probe to minimize the influence of parasitics
- The transient result shows the output voltage in green, the switching signal in purple and the PWM signal in yellow
- The desired output voltage of 1.2 V is achieved and a stable waveform is obtained at a switching frequency of 100 MHz



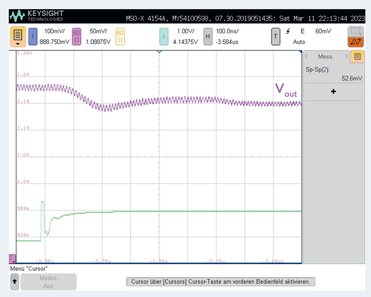
Load Regulation

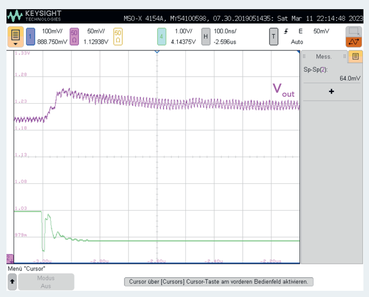
- The output voltage of the prototype was tested under the full load conditions
- The results are shown in the load regulation measurements

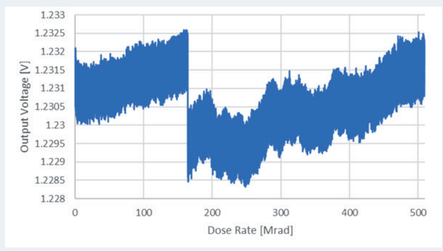


Transient Response

- A settling time of 700 ns and 500 ns was measured for a load change from 0 A to 350 mA and back from 350 mA to 0 A







X-ray (TID)

- The testchip was irradiated with a total ionization dose of 500 Mrad at a dose rate of 2 Mrad/h, performed at -15°C [4]
- The output voltage is plotted against the total dose rate
- The deviation is 4.22 mV, less than 1%

CONCLUSION

A high frequency DC/DC-converter with a stacked switching stage is presented for powering future high energy physics experiments. The DC/DC-converter is built with low voltage core devices to withstand a high dose of irradiation, as core transistors are tolerant to radiation due to their thin gate oxide. By stacking the devices of the switching stage, the DC/DC-converter can be supplied with a four times higher supply voltage. Due to the limited space and high magnetic fields present in the experiments, the converter operates at a frequency of 100 MHz and requires a small air core inductor of 22 nH. Various methods were presented to achieve reliable operation at a maximum load current of 1 A. The prototype demonstrates that a high frequency, stacked DC/DC-converter can withstand the demands of the harsh radiation environment and meet the requirements for increased power efficiency with low mass penalty.

REFERENCES

[1] B. Serneels, M. Steyaert and W. Dehaene, „A 5.5 V SOPA line driver in a standard 1.2 V 0.13 /spl mu/m CMOS technology," Proceedings of the 31st European Solid-State Circuits Conference, 2005. ESSCIRC 2005., 2005, pp. 303-306, doi: 10.1109/ESSCIR.2005.1541620

[2] J. Kampkoetter, M. Karagounis, R. Kokozinski; Design and characterization of a cascode switching stage for high frequency radiation hardened DC/DC converters for the supply of future pixel detectors, 2022 JINST 17 C12022

[3] N. Takai and Y. Fujimura, „Sawtooth generator using two triangular waves" 2008 51st Midwest Symposium on Circuits and Systems, Knoxville, TN, USA, 2008, pp. 706-709

[4] X-ray machine Bonn; https://github.com/SiLab-Bonn/X-ray_machine/wiki