DC Power Circuit Evaluation for the Development of the Barrel Calorimeter Processor (BCP) V2

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- on behalf of the CMS Collaboration -

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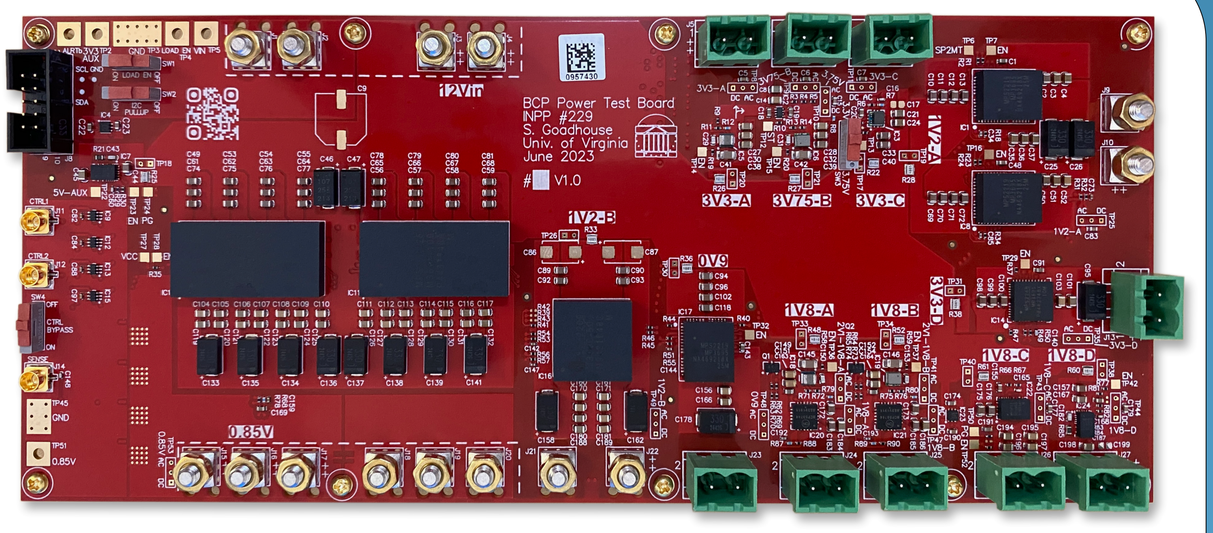
Introduction

The Barrel Calorimeter Processor (BCP) ATCA blade will be the core board of the off-detector electronics for the HL-LHC CMS barrel calorimeters. It will host a Xilinx Virtex UltraScale+ high-performance FPGA along with up to 18 FireFly optical transceivers with a bit rate up to 25 Gbps. The power needs of the BCP will be challenging to meet with nearly 160W of power for the FPGA core while also providing 45W of ultra-low noise power for the FPGA high-speed transceivers, 45W of low noise power for the FireFly and another 50W for microcontrollers and other support electronics on the BCP. In order to evaluate the performance of the power circuits for the BCP, a Power Test Board was designed with the chosen circuits that were available with today's supply chain shortages in a configuration suitable for the BCP. This test board allows for experimentation with multiple circuit choices in a less expensive board that is more conducive to a laboratory environment.

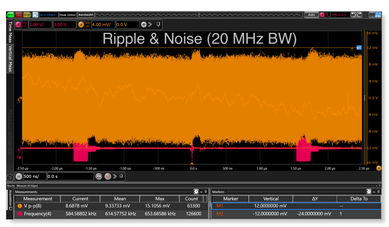


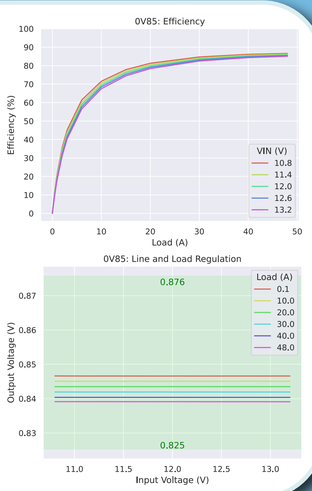
Power Test Board

FPGA Core Voltage
Dual MPM3695-100

0V85

	Required	Measured	Pass?
Voltage (V)	0.825 - 0.876	0.839 - 0.847	✓
Max Load (A)	187	48	?
Noise (mVpp)	< 34	24	✓

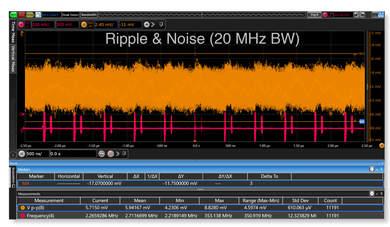


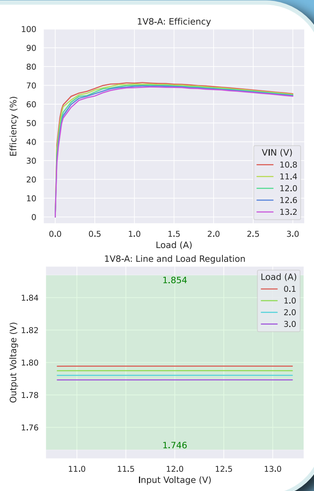


Clock Generation
TPS82130 + NCP59744

1V8-A

	Required	Measured	Pass?
Voltage (V)	1.746 - 1.854	1.789 - 1.798	✓
Max Load (A)	2.1	3.0	✓
Noise (mVpp)	< 100	10	✓

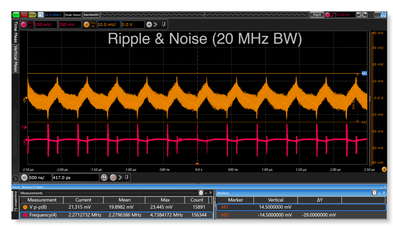


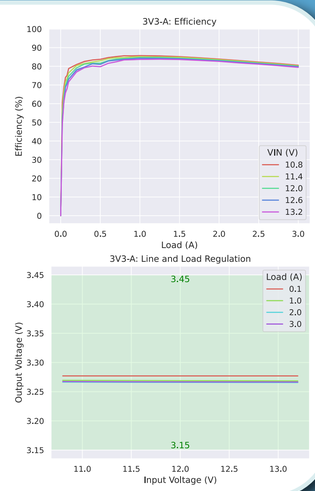


Clock Gen. & SSD
TPS82130

3V3-A

	Required	Measured	Pass?
Voltage (V)	3.150 - 3.450	3.265 - 3.277	✓
Max Load (A)	2.8	3.0	✓
Noise (mVpp)	< 100	28	✓

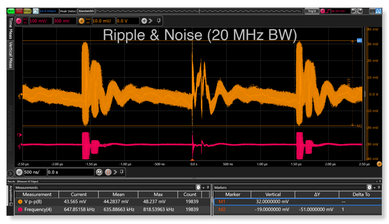


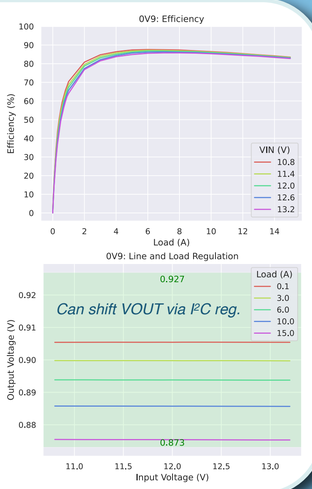


FPGA MGT Core
MPM3695-25

0V9

	Required	Measured	Pass?
Voltage (V)	0.873 - 0.927	0.875 - 0.905	✓
Max Load (A)	15	15	✓
Noise (mVpp)	< 10	50	✗

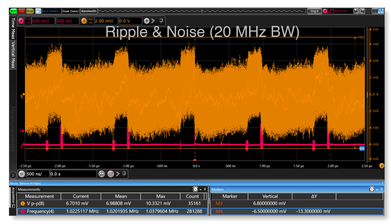


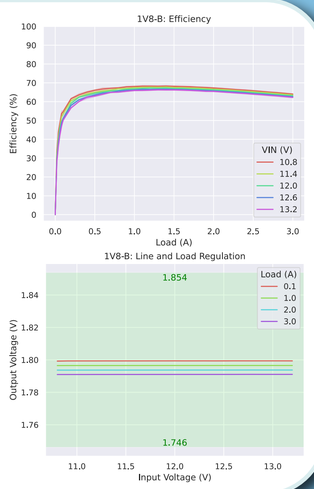


Clock Generation *(alt.)*
MUN12AD03 + NCP59744

1V8-B

	Required	Measured	Pass?
Voltage (V)	1.746 - 1.854	1.791 - 1.799	✓
Max Load (A)	2.1	3.0	✓
Noise (mVpp)	< 100	12	✓

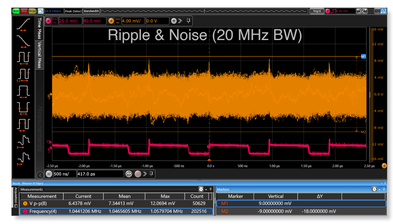


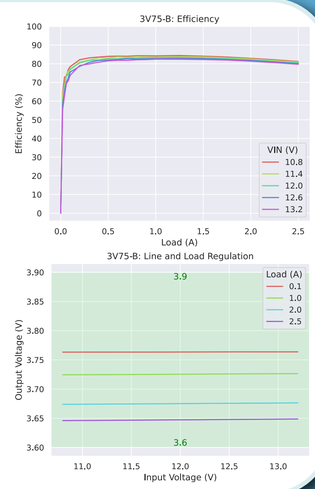


FireFly 25G TX VCSEL
MUN12AD03

3V75-B

	Required	Measured	Pass?
Voltage (V)	3.600 - 3.900	3.646 - 3.764	✓
Max Load (A)	1.7	2.5	✓
Noise (mVpp)	< 50	18	✓

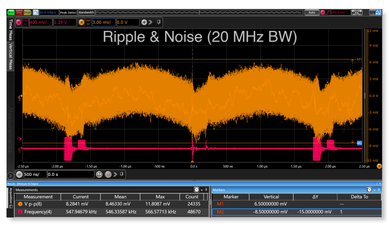


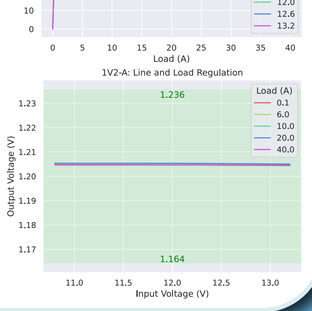


FPGA MGT Term.
Dual MPM3695-25

1V2-A

	Required	Measured	Pass?
Voltage (V)	1.164 - 1.236	1.204 - 1.205	✓
Max Load (A)	26	40	✓
Noise (mVpp)	< 10	12	✗

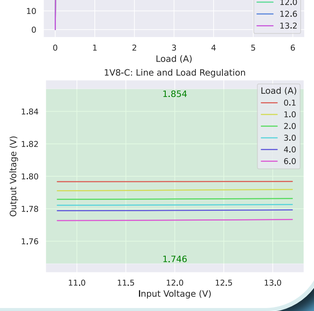




FPGA VCCAux, FireFly
MPM3650C

1V8-C

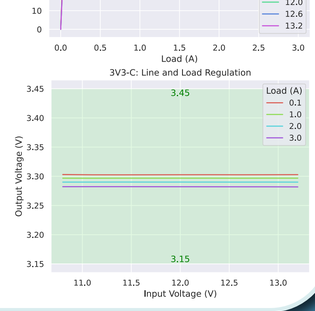
	Required	Measured	Pass?
Voltage (V)	1.746 - 1.854	1.773 - 1.797	✓
Max Load (A)	4.0	6.0	✓
Noise (mVpp)	< 54	25	✓



Clock Gen. & SSD
MPM3632S

3V3-C

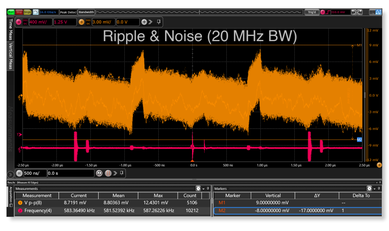
	Required	Measured	Pass?
Voltage (V)	3.150 - 3.450	3.282 - 3.304	✓
Max Load (A)	2.8	3.0	✓
Noise (mVpp)	< 100	41	✓

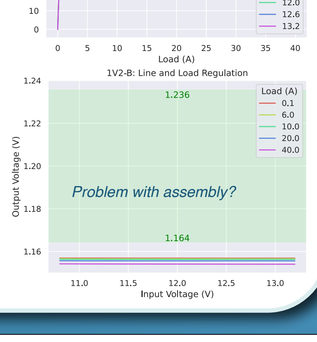


FPGA MGT Term. *(alt.)*
MPM3690-50B

1V2-B

	Required	Measured	Pass?
Voltage (V)	1.164 - 1.236	1.154 - 1.157	✗
Max Load (A)	26	40	✓
Noise (mVpp)	< 10	13	✗

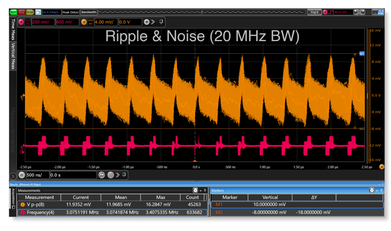


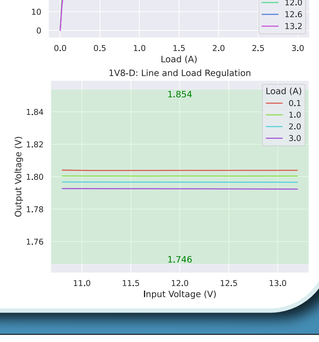


Clock Generation *(alt.)*
MPM3632C

1V8-D

	Required	Measured	Pass?
Voltage (V)	1.746 - 1.854	1.792 - 1.805	✓
Max Load (A)	2.1	3.0	✓
Noise (mVpp)	< 100	18	✓

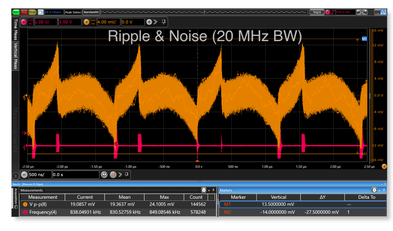


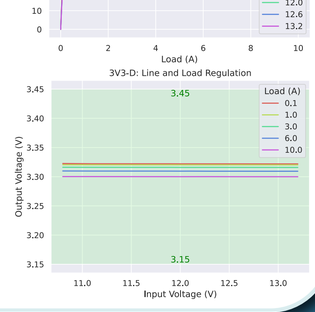


ELM I/O & FireFly *(alt.)*
MPM3695-10

3V3-D

	Required	Measured	Pass?
Voltage (V)	3.150 - 3.450	3.300 - 3.324	✓
Max Load (A)	4.0	10	✓
Noise (mVpp)	< 50	27	✓





Conclusions

The 3V75, 3V3 and 1V8 circuits all meet requirements but the 0V9 and 1V2 circuits need linear regulators on the output in order to reduce the noise below required levels. Additional equipment is needed in order to fully test the load capacity of the 0V85 circuit.

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